FIG. 1

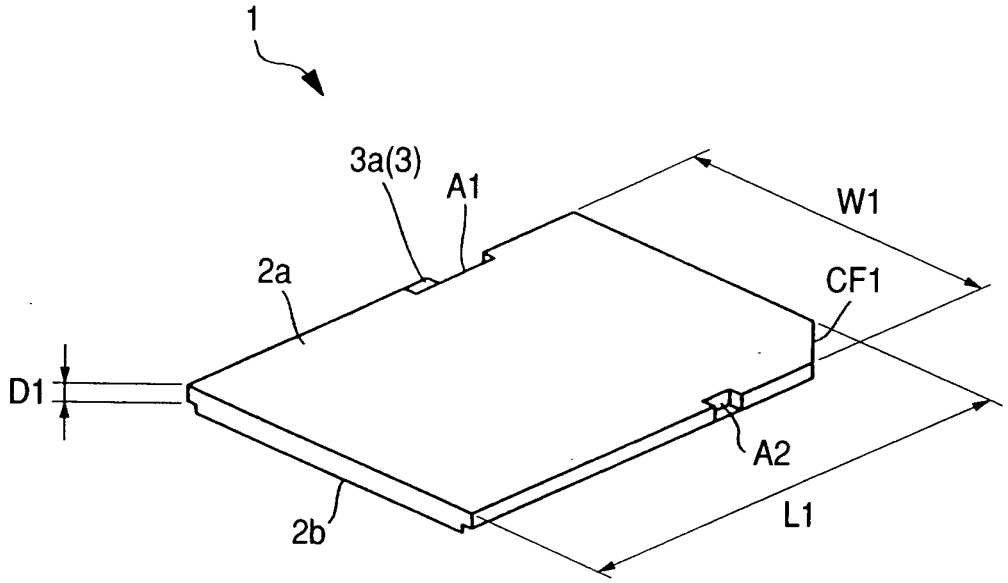


FIG. 2(a)

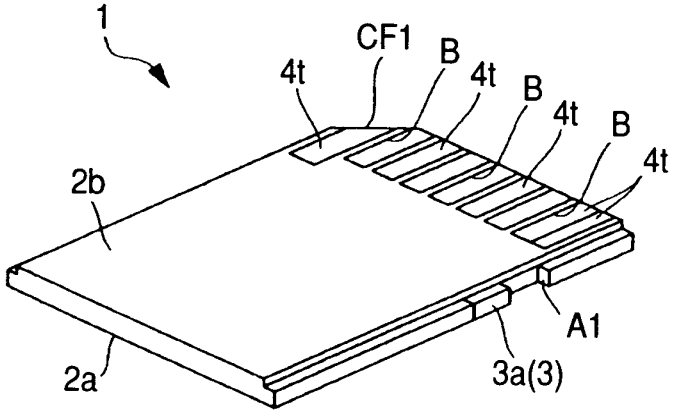


FIG. 2(b)

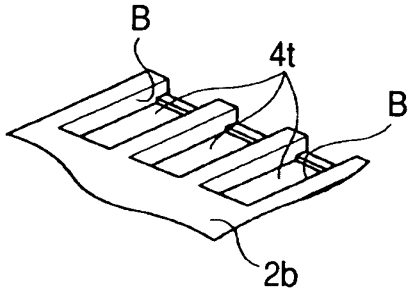


FIG. 3

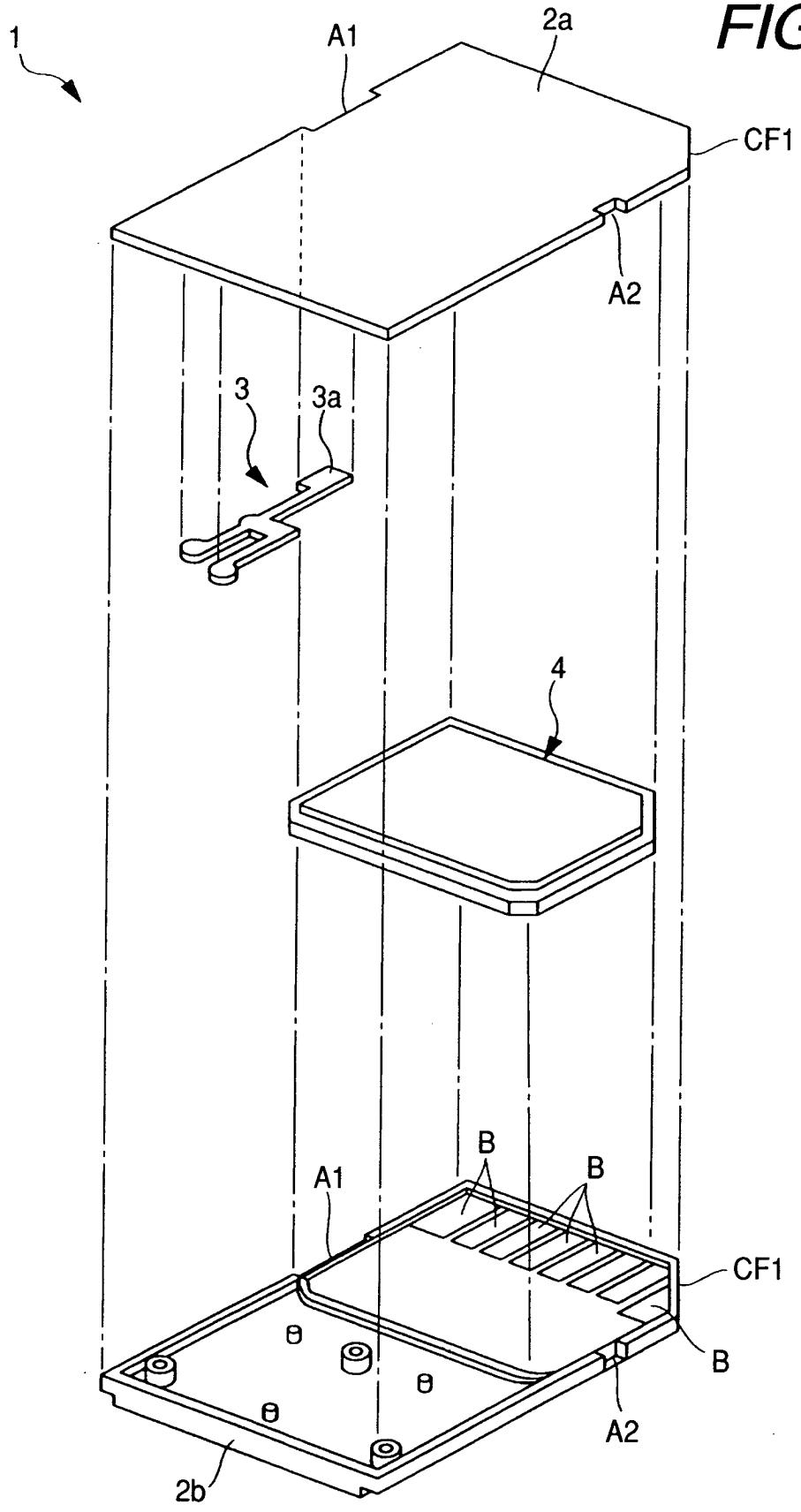
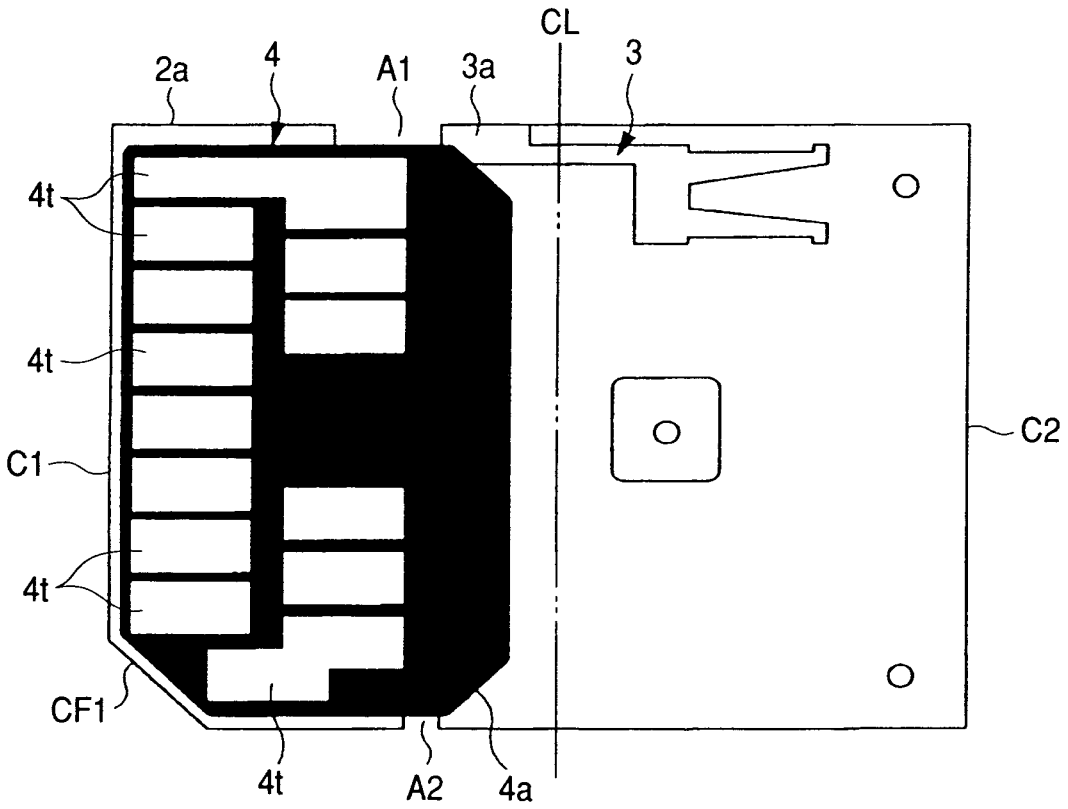


FIG. 4



2a: FIRST CASE
3: SWITCH
4: MEMORY BODY (IC BODY)
4a: WIRING SUBSTRATE
4t: EXTERNAL CONNECTING TERMINAL

C1: FIRST END SIDE
C2: SECOND END SIDE
CL: MIDLINE

FIG. 5

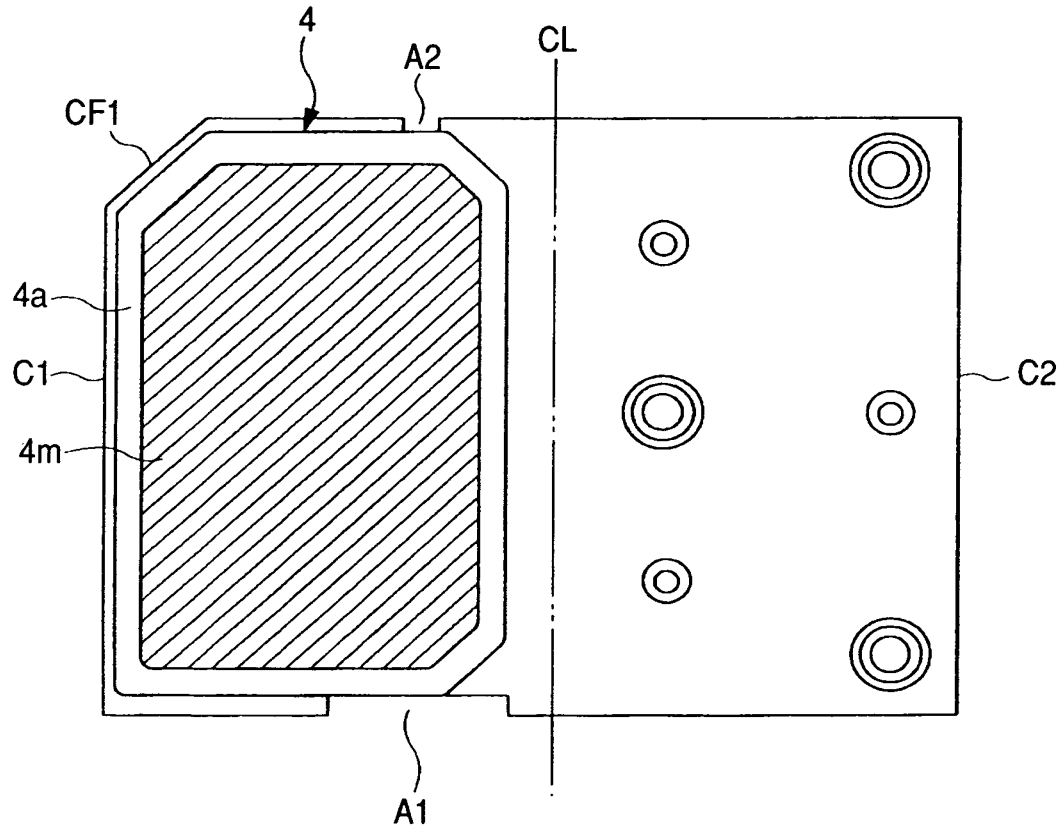


FIG. 6

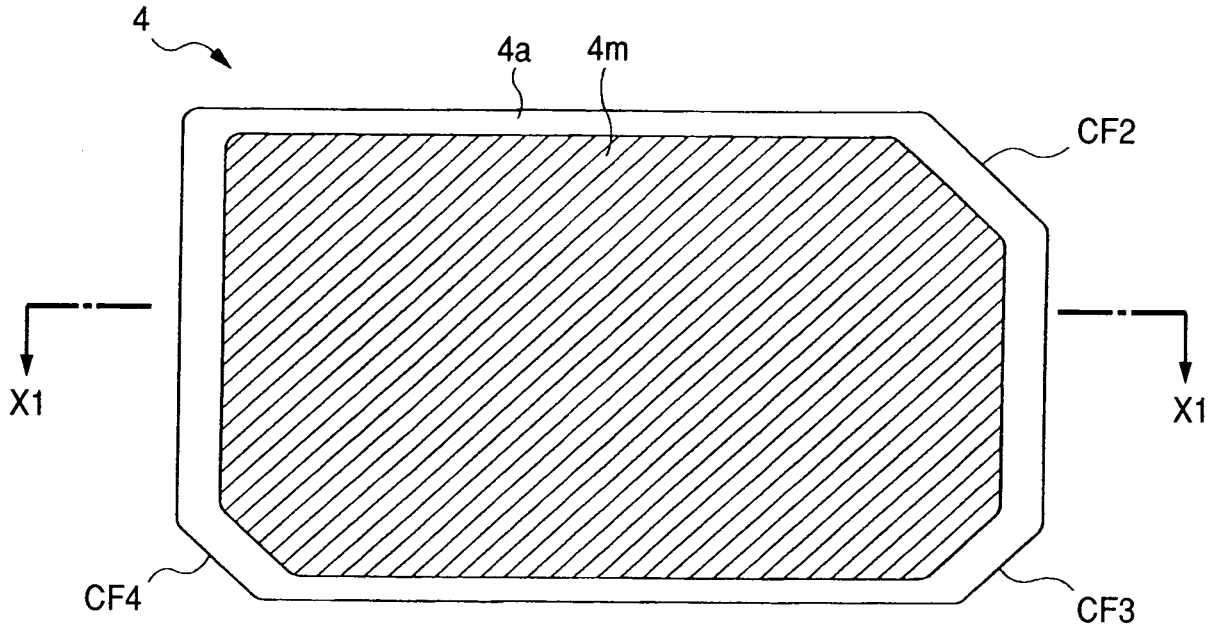


FIG. 7

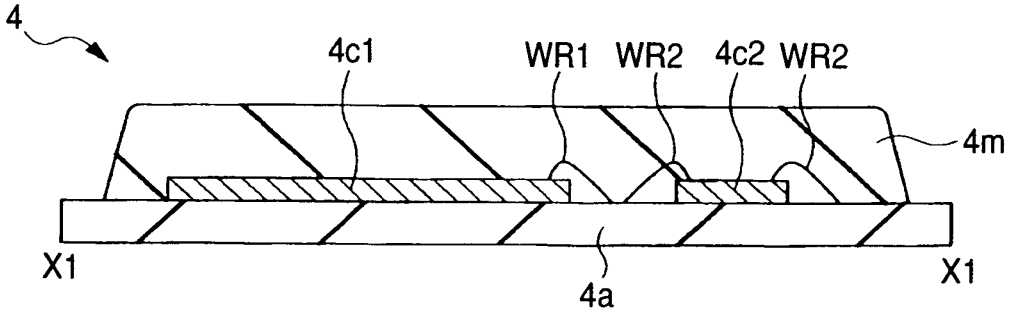


FIG. 8

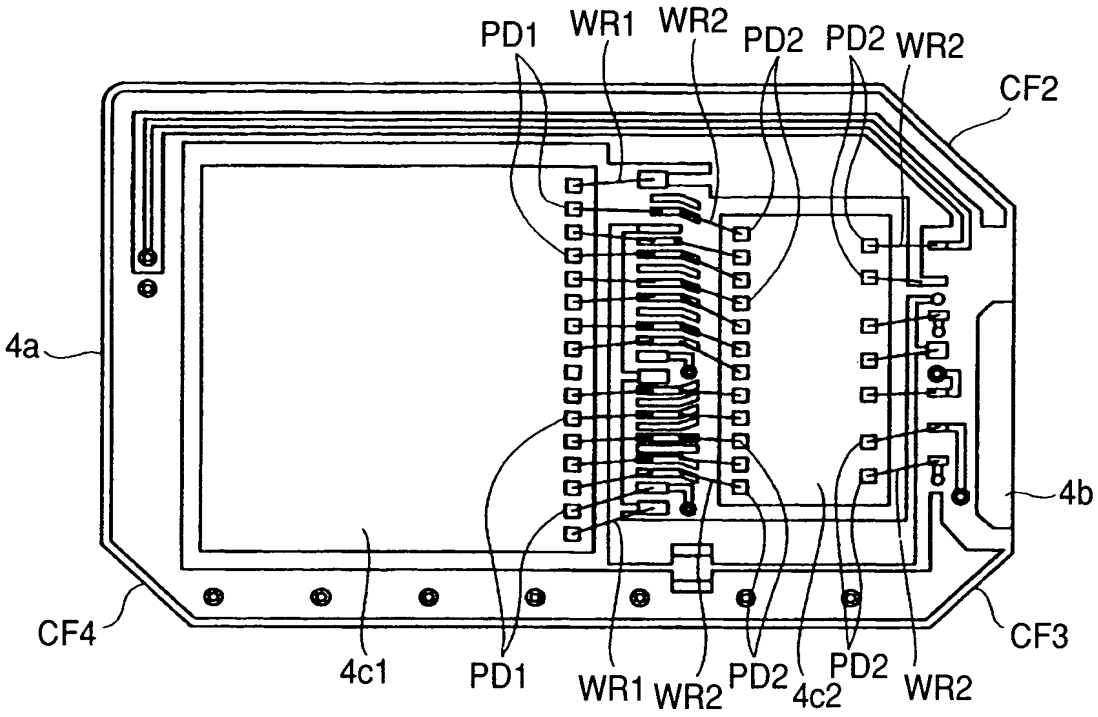

PD1
WR1
WR2
PD2
PD2
WR2
CF2
4a
4b
CF4
CF3
4c1
PD1
WR1
WR2
PD2
4c2
PD2
WR2

FIG. 9

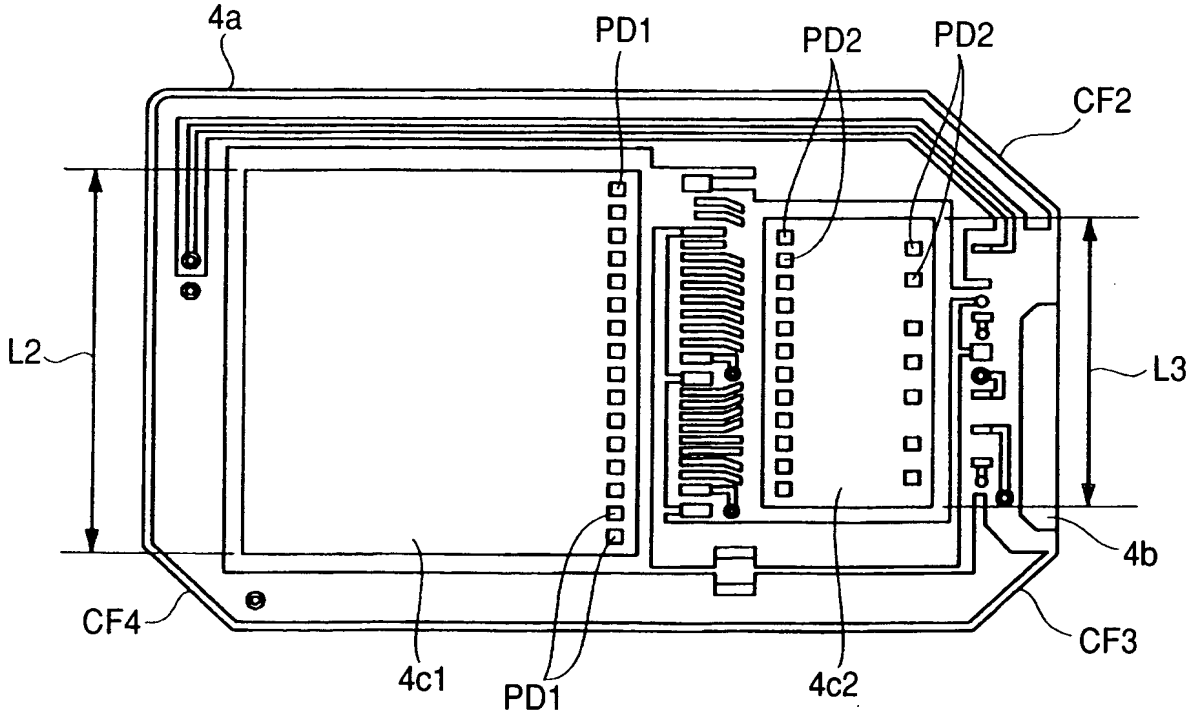

4a
PD1
PD2
PD2
CF2
L2
L3
4b
CF4
CF3
4c1
PD1
4c2

FIG. 10

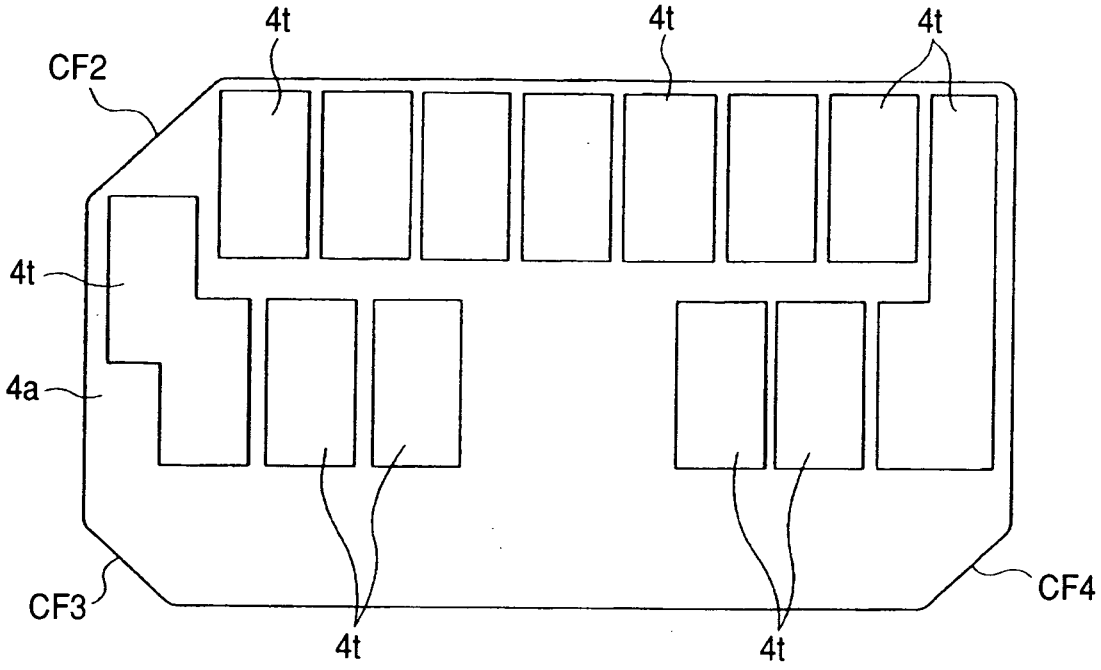


FIG. 11

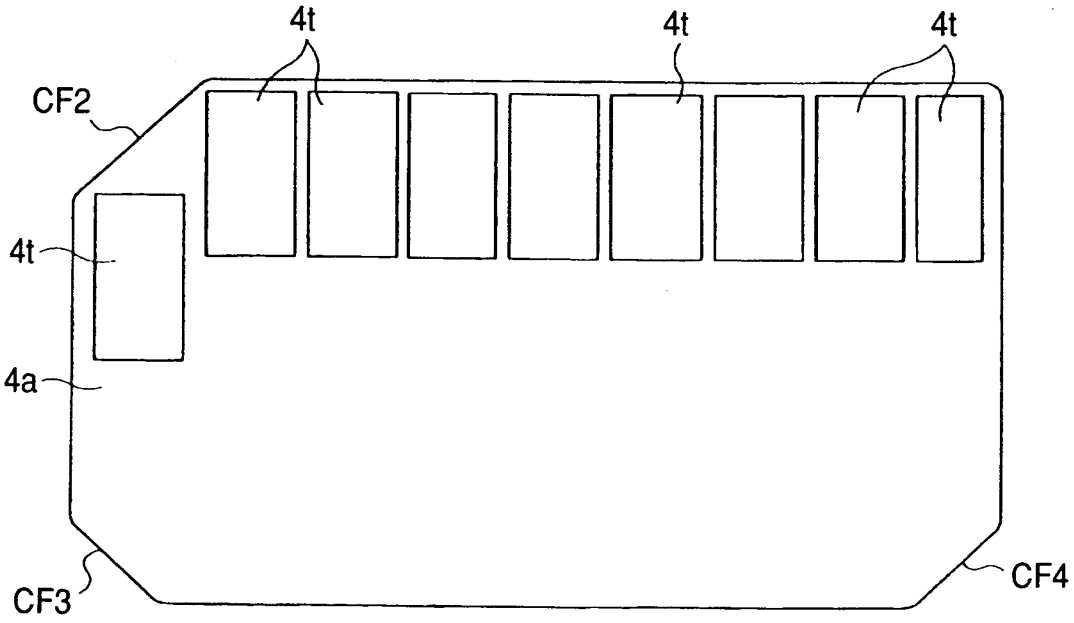


FIG. 12

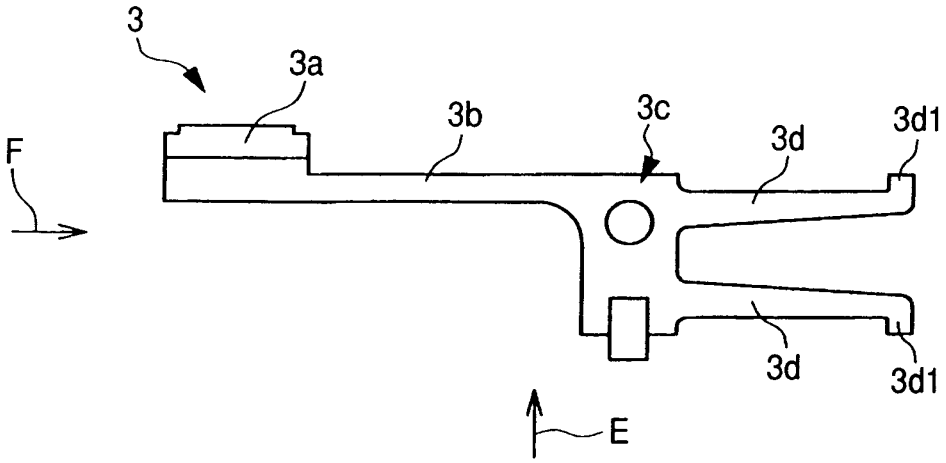


FIG. 13

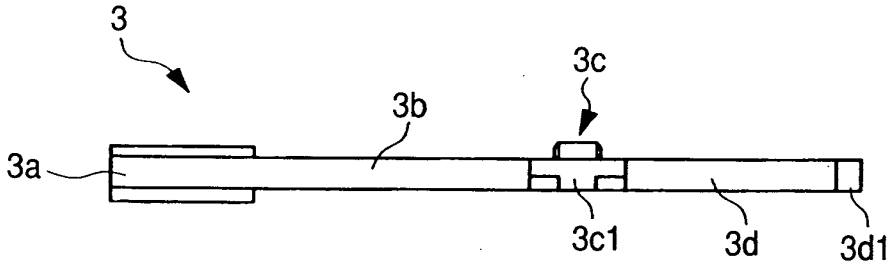


FIG. 14

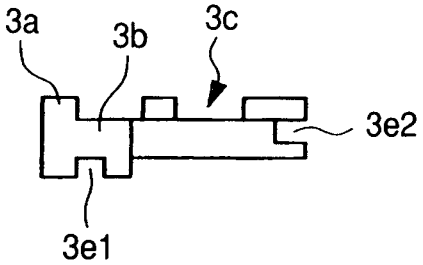


FIG. 15

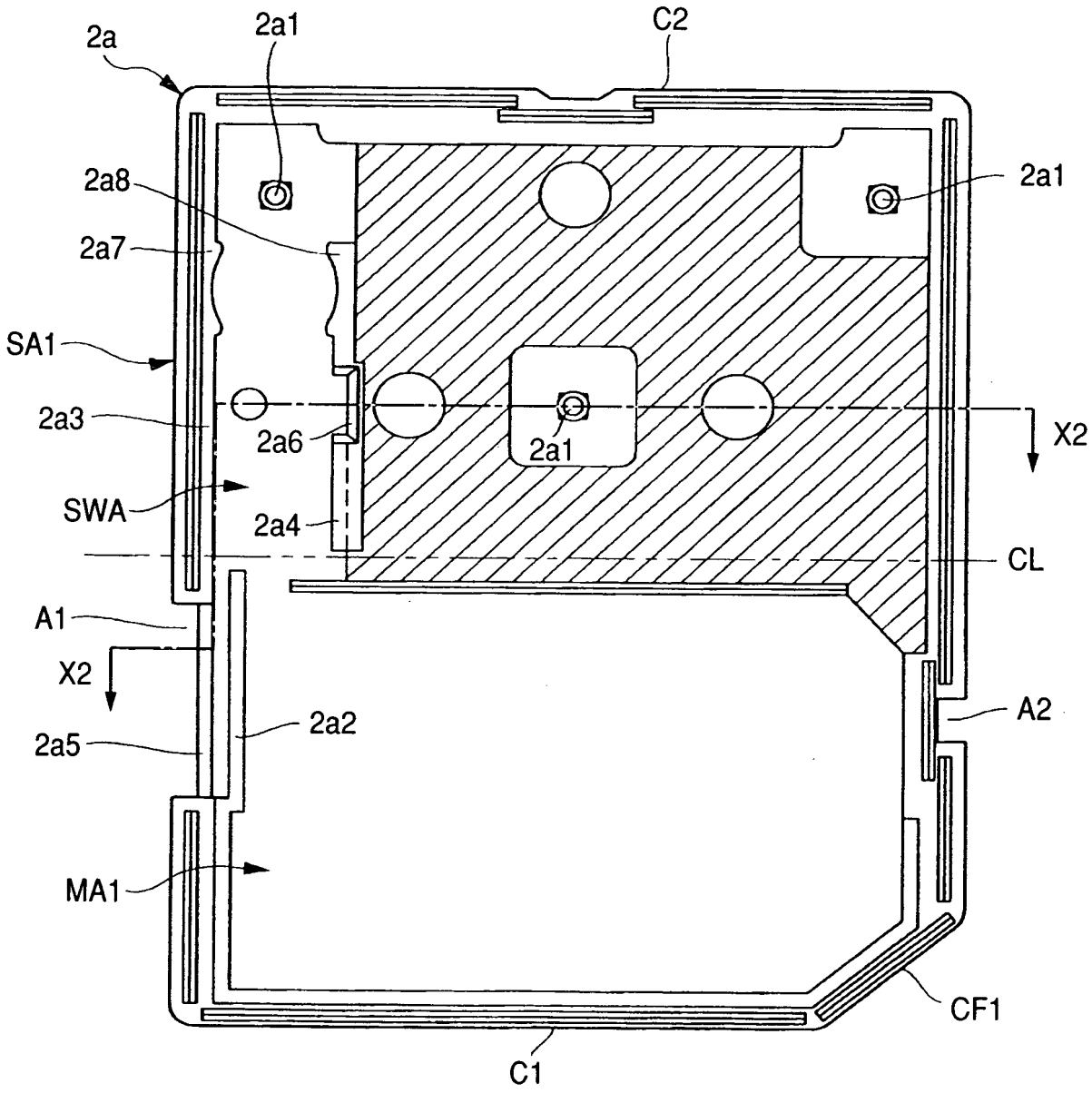

2a
2a1
C2
2a8
2a1
2a7
SA1
2a3
2a6
2a1
X2
SWA
2a4
CL
A1
X2
2a2
A2
2a5
MA1
CF1
C1

FIG. 16

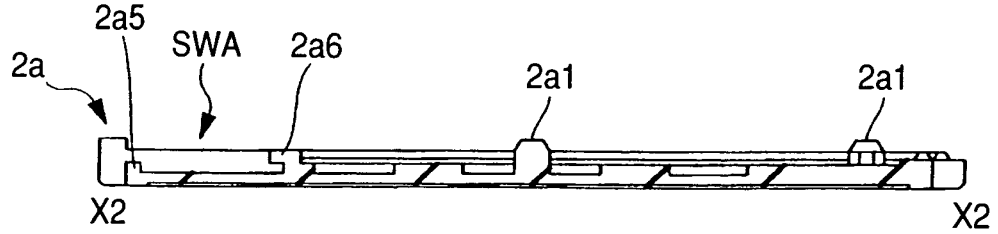

2a5
SWA
2a6
2a
2a1
2a1
X2
X2

FIG. 17

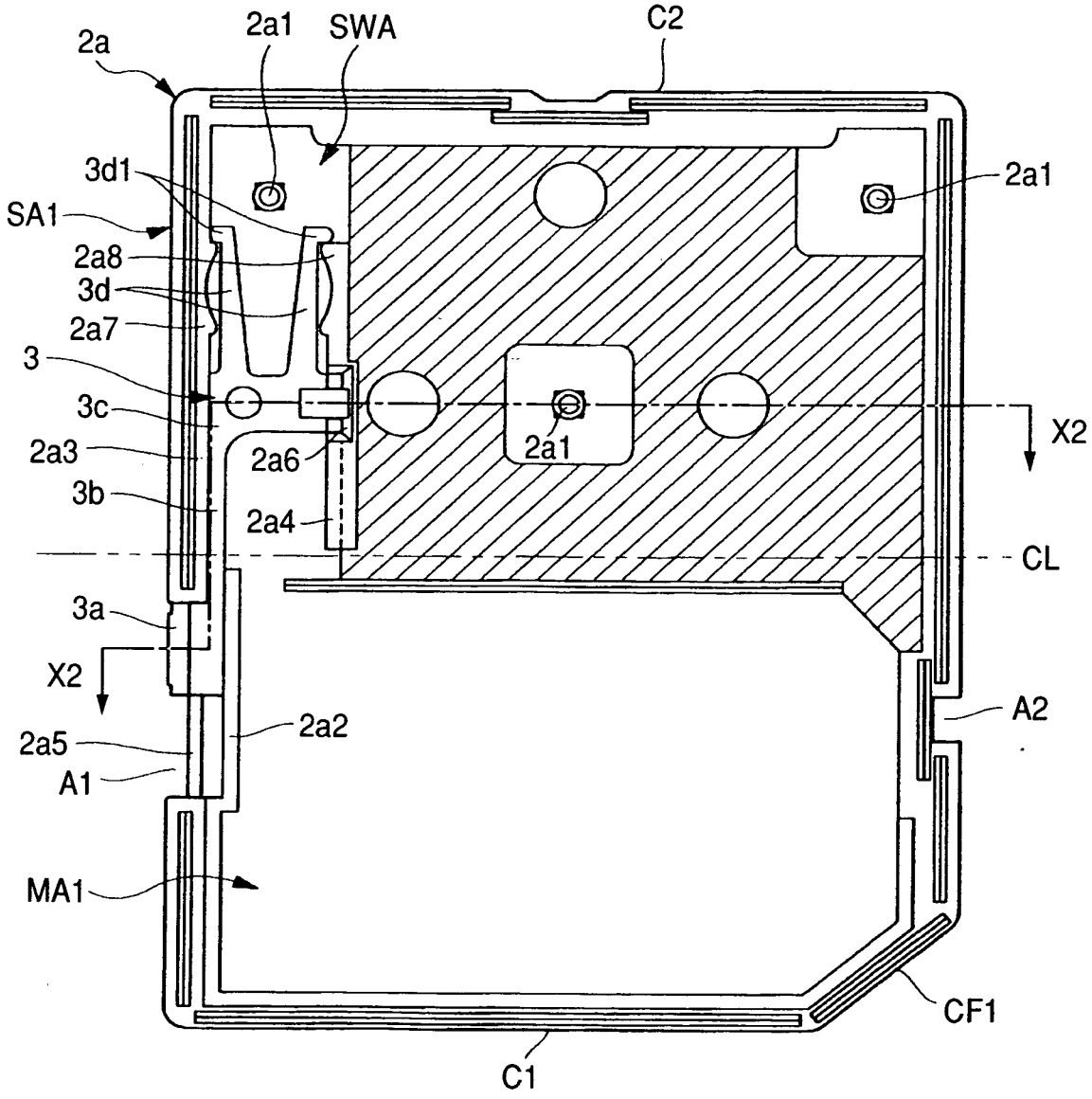

2a
2a1
SWA
C2
3d1
2a1
SA1
2a8
3d
2a7
3
3c
2a3
3b
2a6
2a4
2a1
X2
CL
3a
X2
2a5
A1
2a2
A2
MA1
CF1
C1

FIG. 18

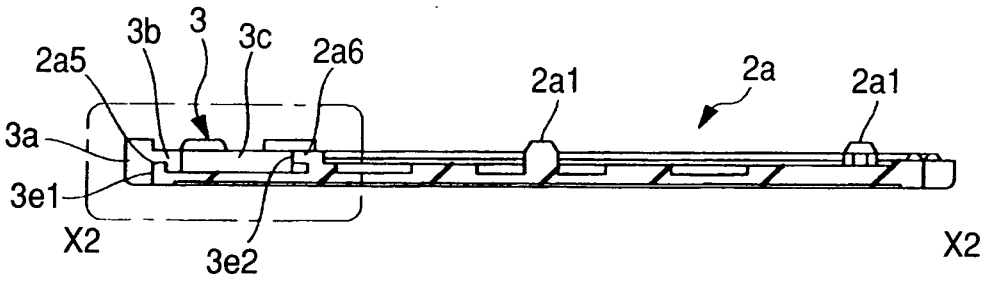

3b
3
3c
2a5
2a6
2a1
2a
2a1
3a
3e1
X2
3e2
X2

FIG. 19

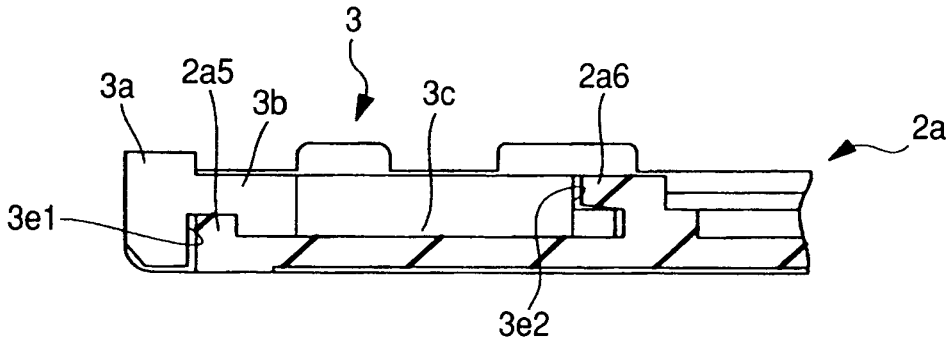

3
3a
2a5
3b
3c
2a6
2a
3e1
3e2

FIG. 20

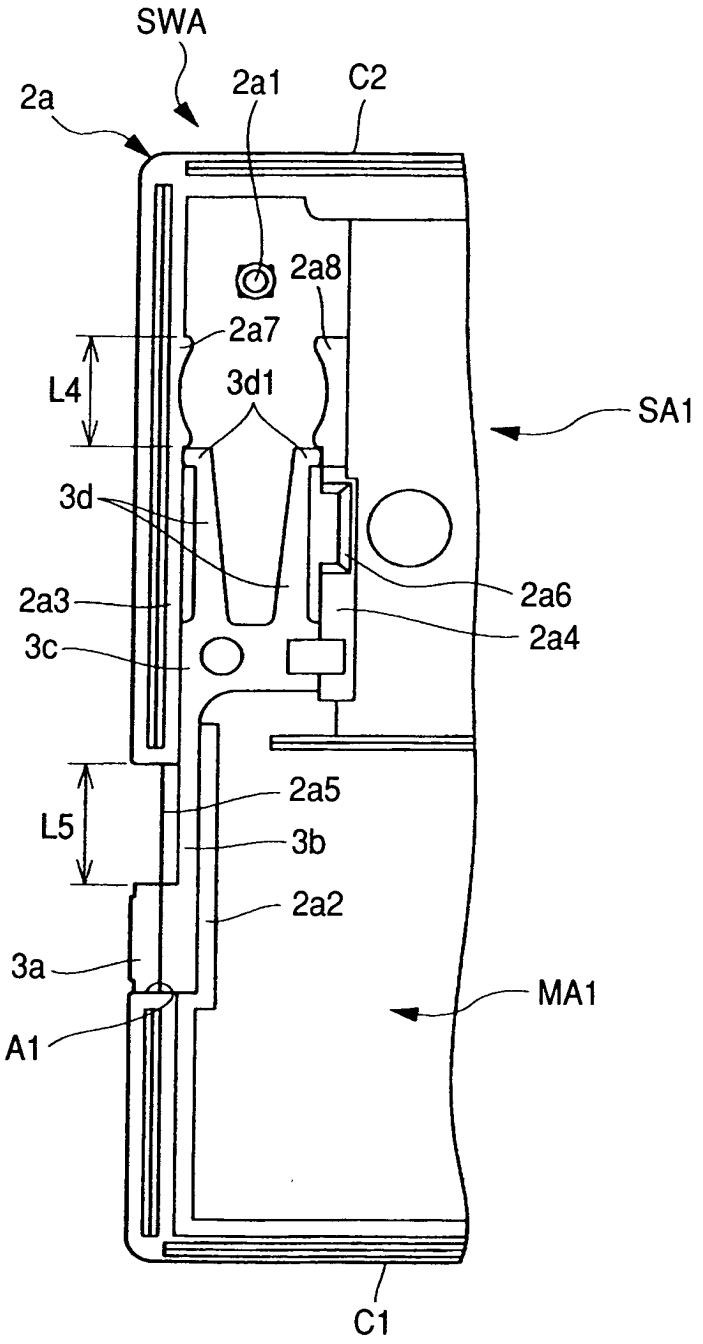

SWA
2a
2a1
C2
2a8
2a7
L4
3d1
SA1
3d
2a3
2a6
2a4
3c
2a5
L5
3b
2a2
3a
MA1
A1
C1

FIG. 21

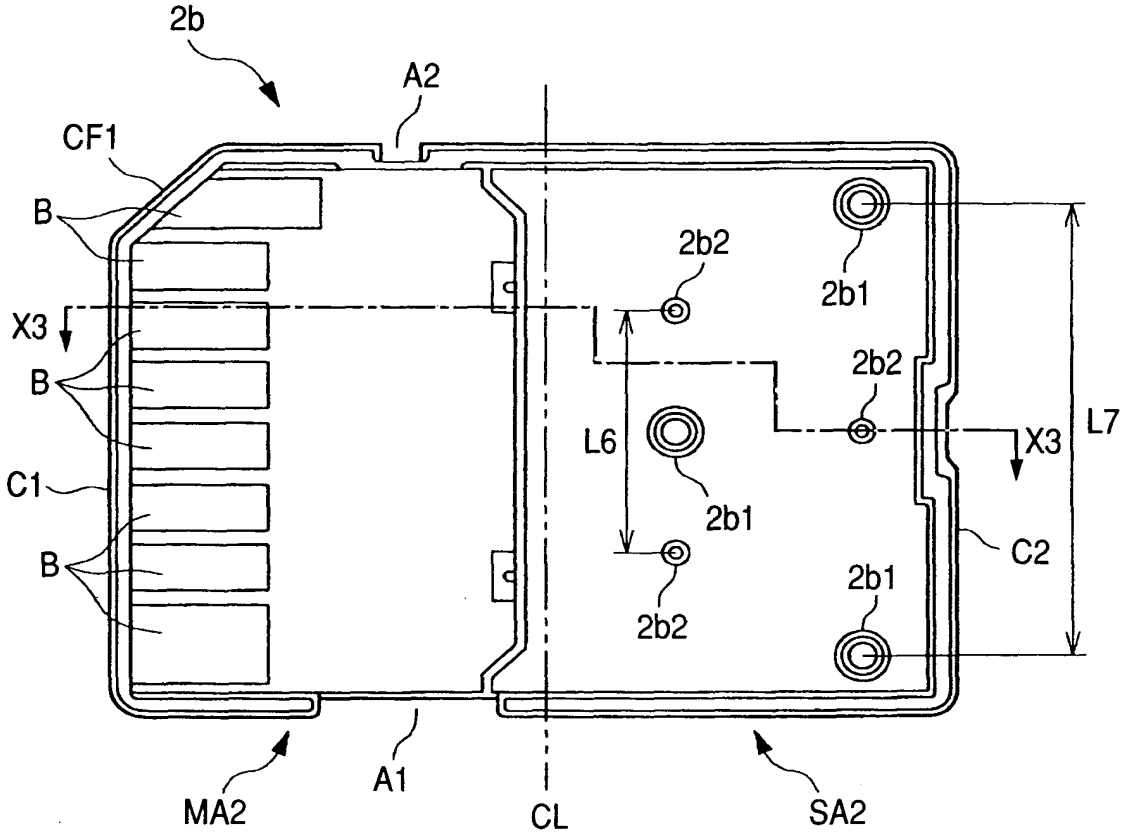

2b
A2
CF1
B
X3
B
C1
B
2b2
2b1
L6
2b1
2b2
2b2
X3
L7
C2
2b1
MA2
A1
CL
SA2

FIG. 22

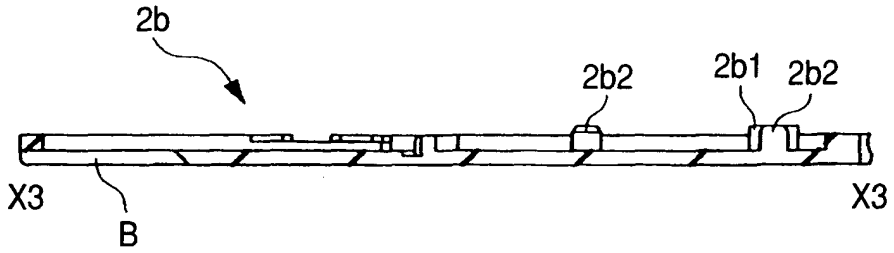

2b
2b2
2b1
2b2
X3
B
X3

FIG. 23

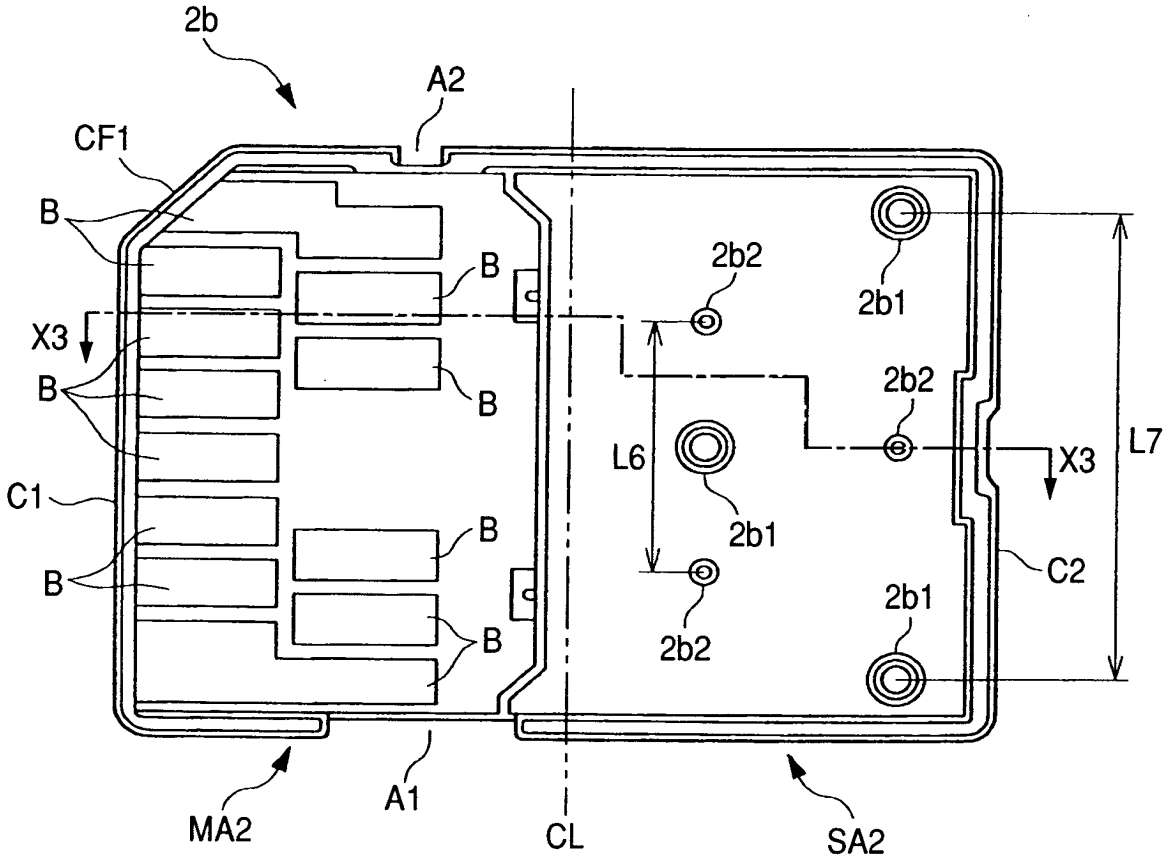

2b
A2
CF1
B
B
X3
B
B
C1
B
B
B
B
2b2
2b1
2b2
L6
2b1
X3
L7
C2
2b1
2b2
MA2
A1
CL
SA2

FIG. 24

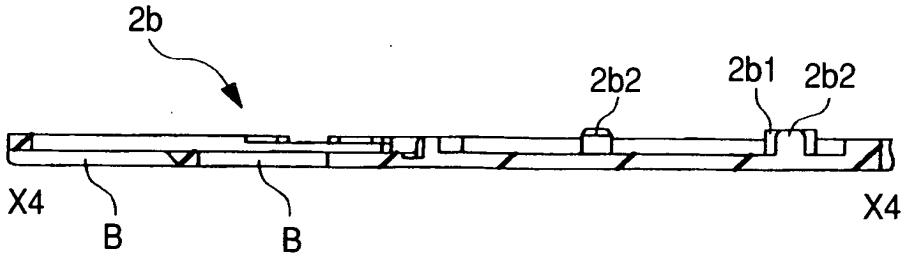

2b
2b2
2b1
2b2
X4
B
B
X4

FIG. 25

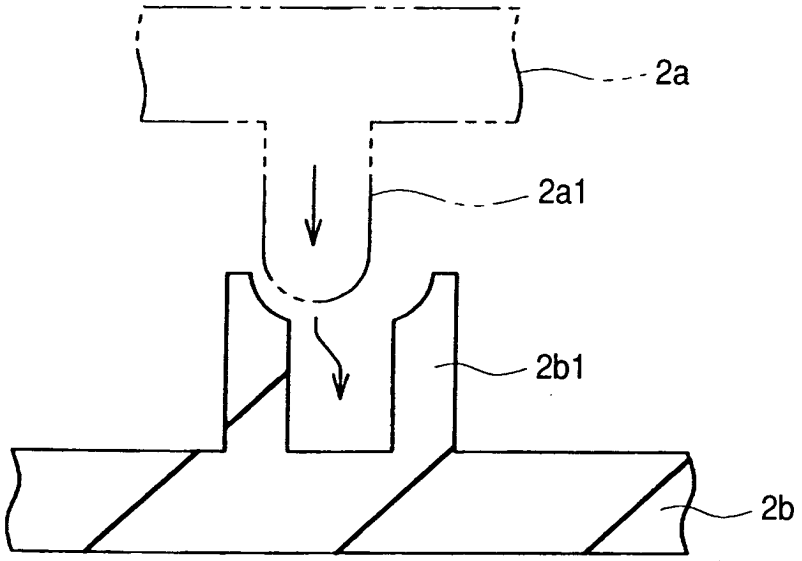


FIG. 26

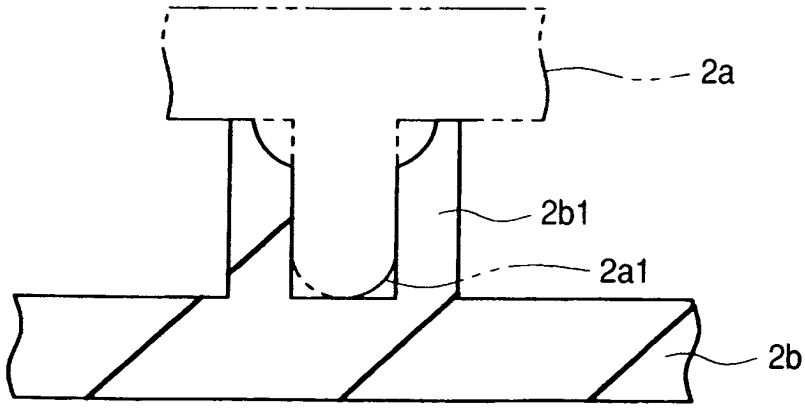


FIG. 27

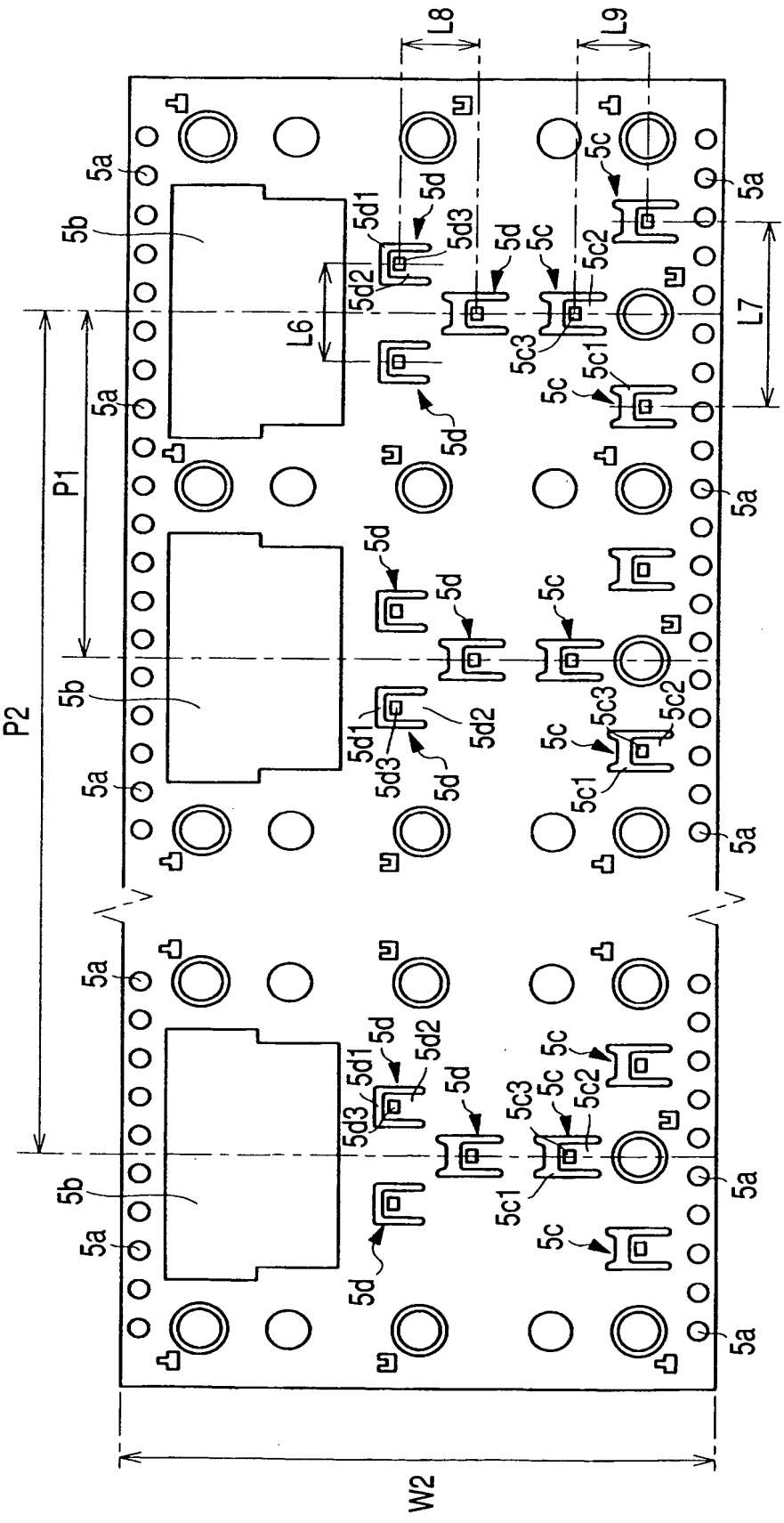


FIG. 28

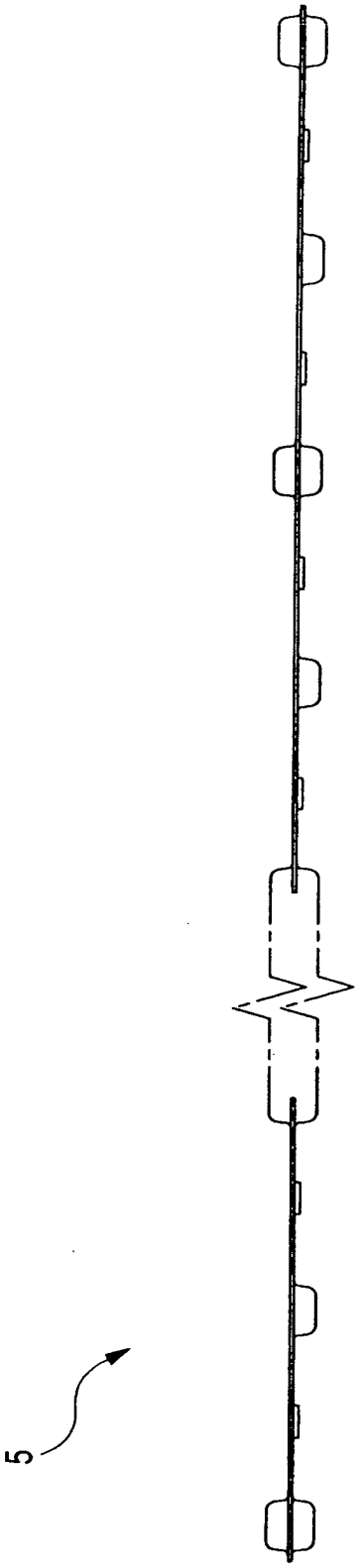


FIG. 29

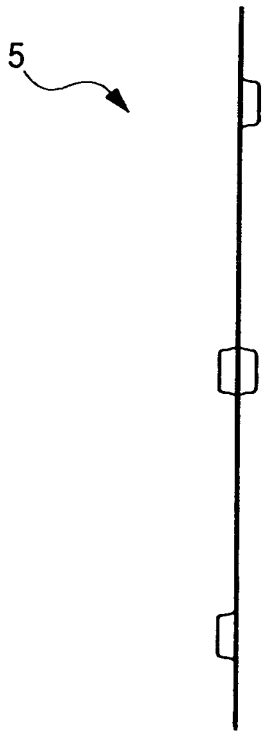


FIG. 30

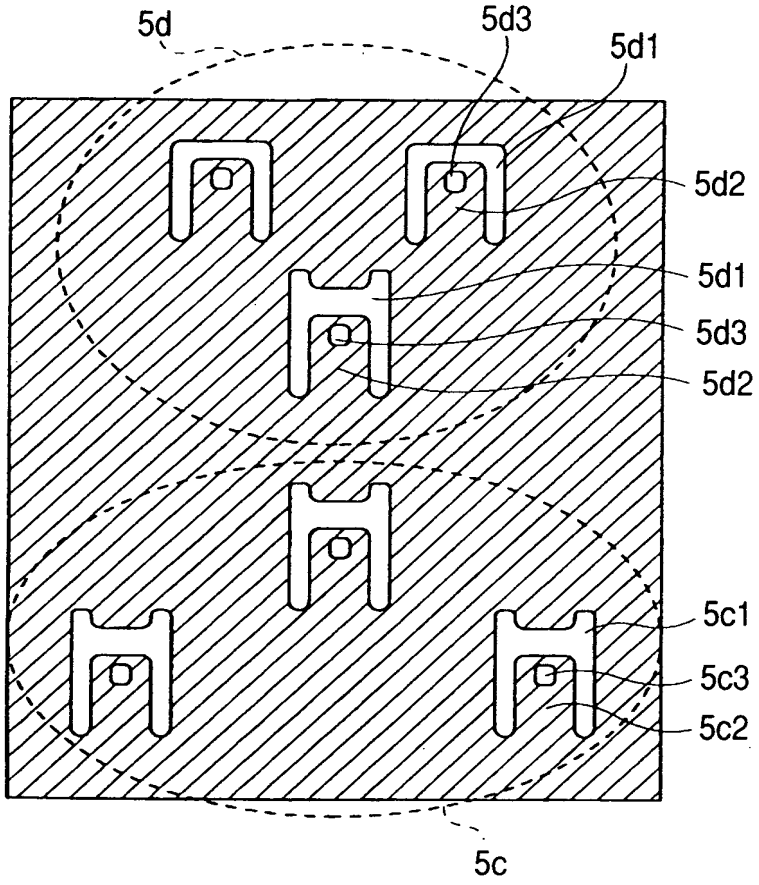


FIG. 31

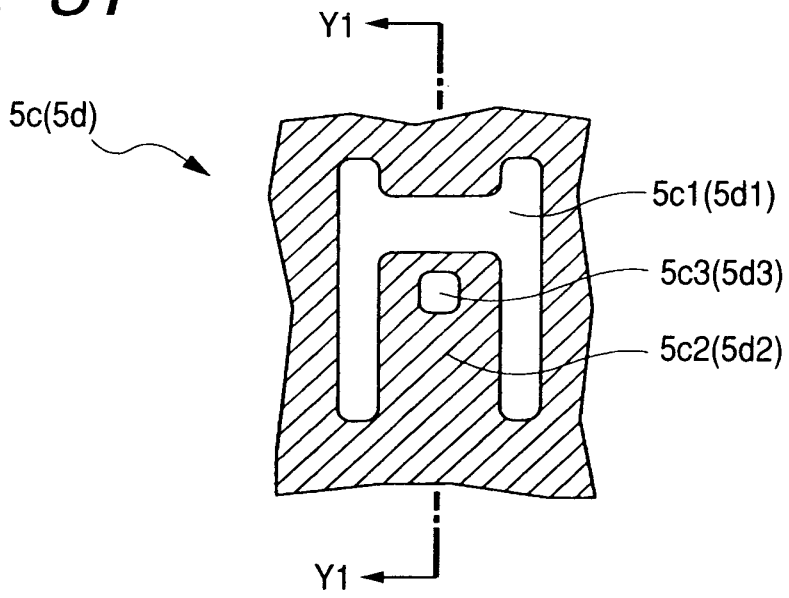


FIG. 32

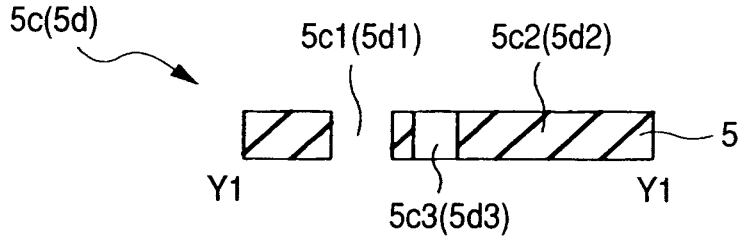


FIG. 33

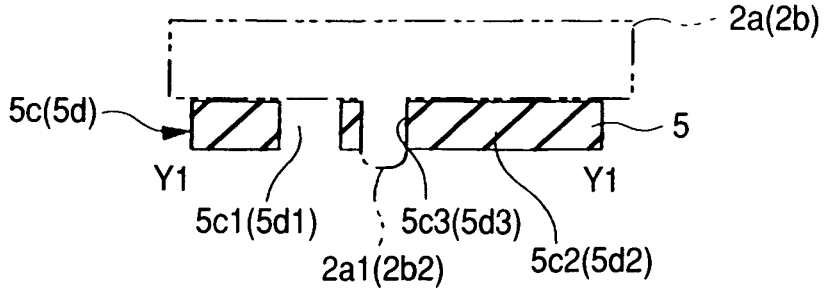


FIG. 34

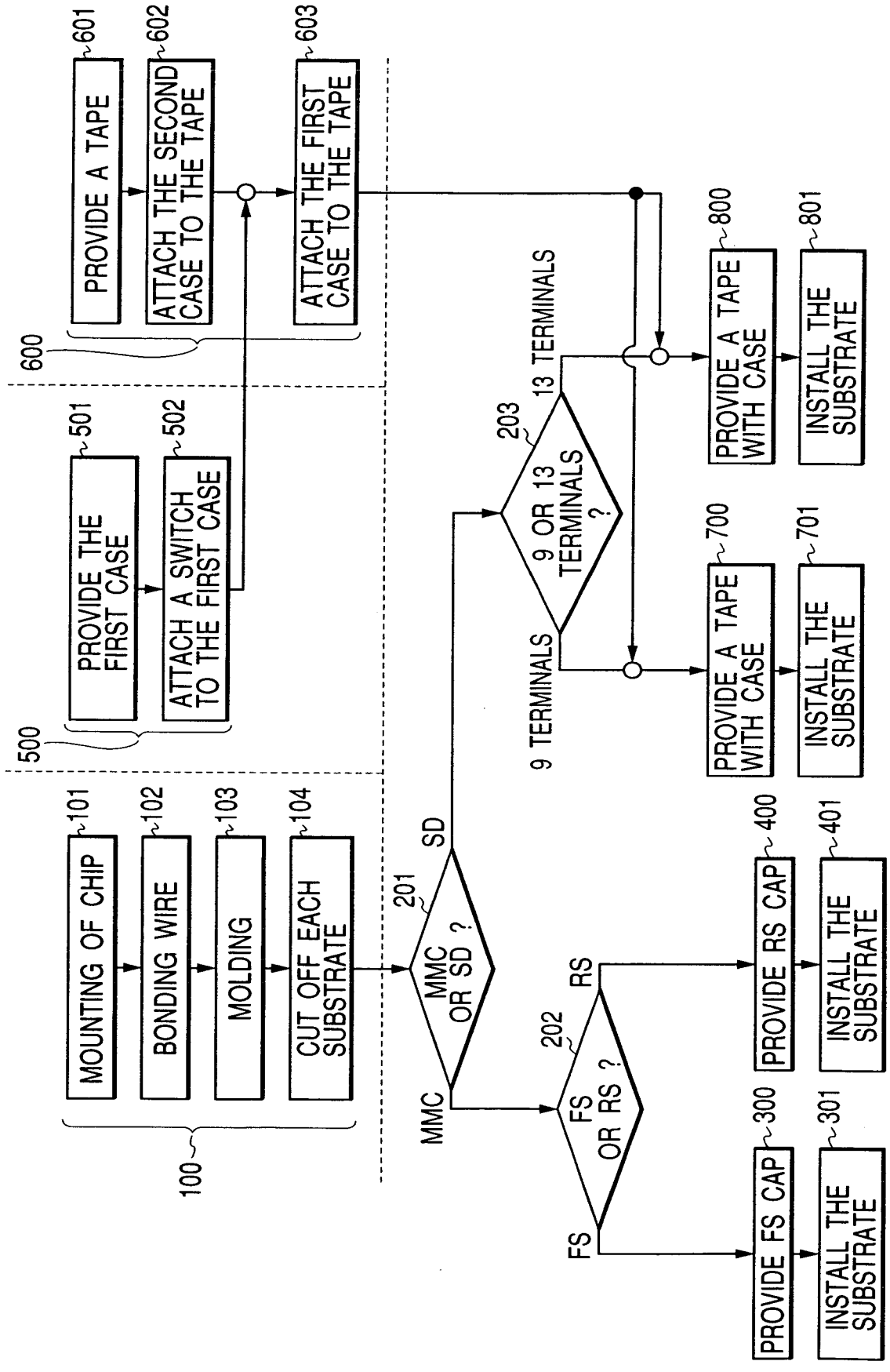

MOUNTING OF CHIP
101
BONDING WIRE
102
MOLDING
103
CUT OFF EACH SUBSTRATE
104
100
PROVIDE THE FIRST CASE
501
ATTACH A SWITCH TO THE FIRST CASE
502
500
PROVIDE A TAPE
601
ATTACH THE SECOND CASE TO THE TAPE
602
ATTACH THE FIRST CASE TO THE TAPE
603
600
MMC OR SD ?
201
SD
MMC
FS OR RS ?
202
RS
FS
9 OR 13 TERMINALS ?
203
13 TERMINALS
9 TERMINALS
PROVIDE RS CAP
400
INSTALL THE SUBSTRATE
401
PROVIDE FS CAP
300
INSTALL THE SUBSTRATE
301
PROVIDE A TAPE WITH CASE
700
INSTALL THE SUBSTRATE
701
PROVIDE A TAPE WITH CASE
800
INSTALL THE SUBSTRATE
801

FIG. 35

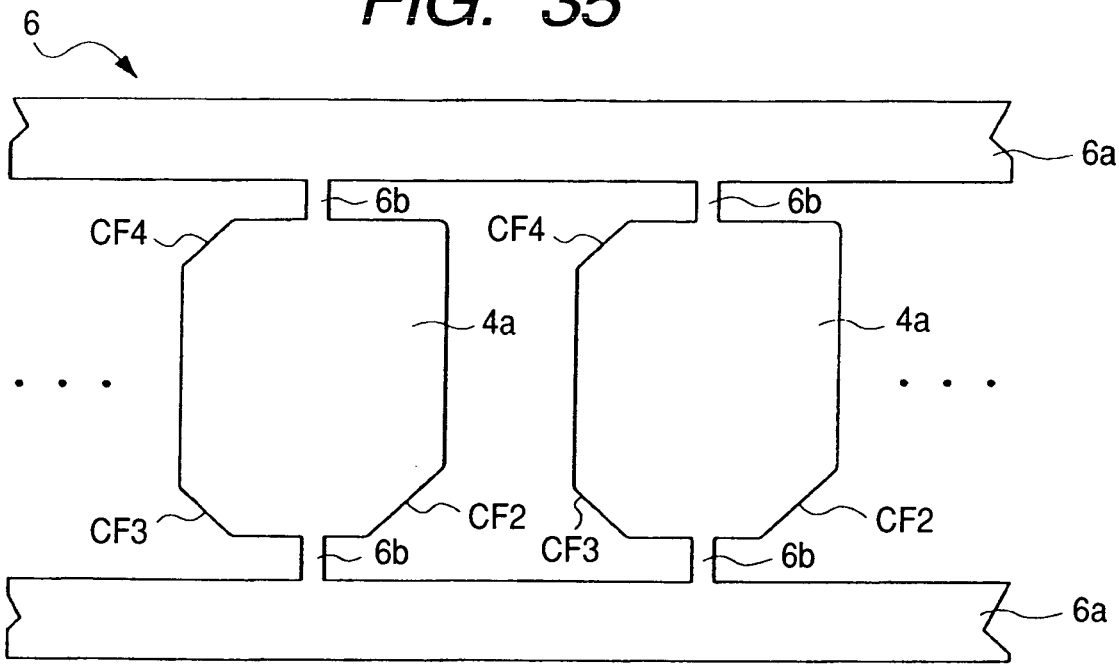

6
6a
6b
CF4
4a
CF2
CF3
6b
6a

FIG. 36

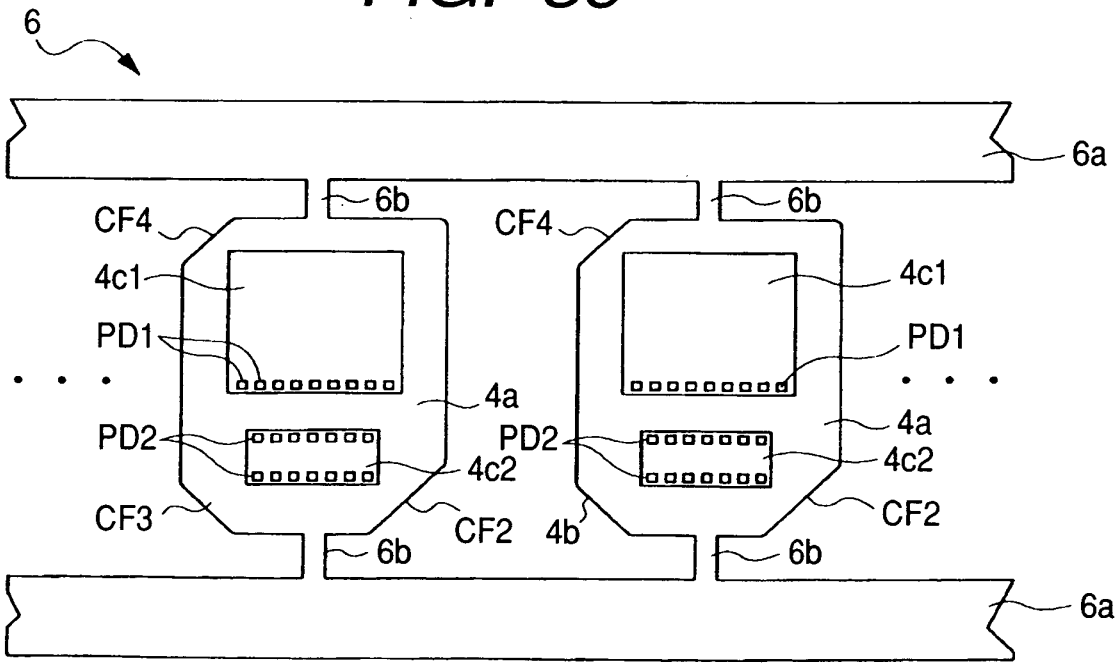

6
6a
6b
CF4
4c1
PD1
4a
PD2
4c2
CF3
CF2
4b
6b
6a

FIG. 37

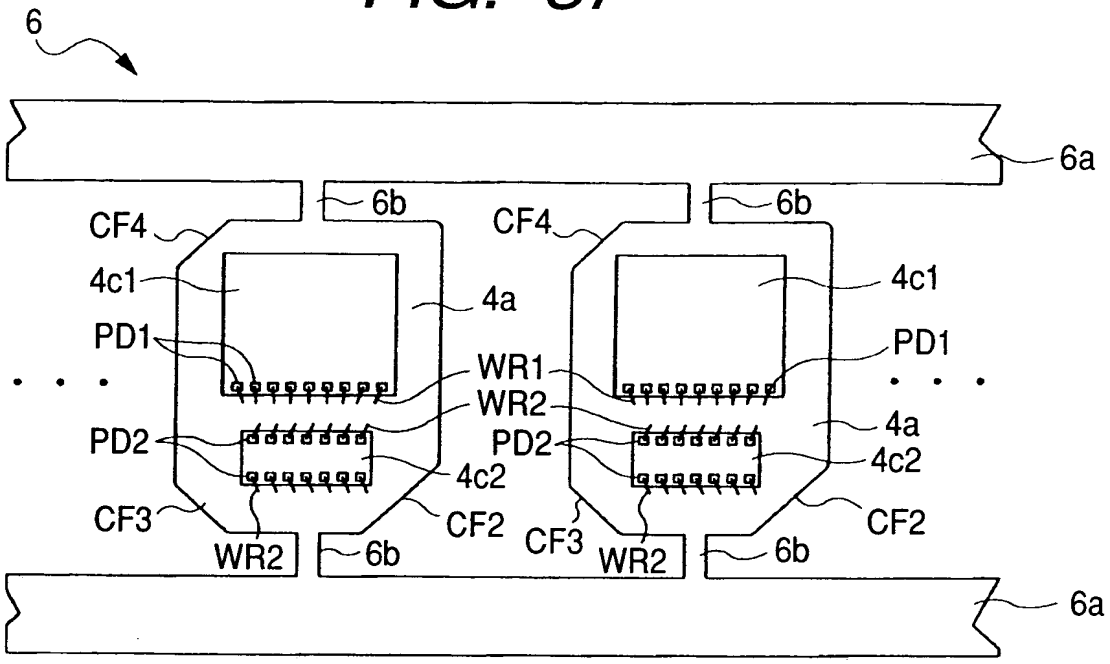

6
6a
6b
CF4
4c1
4a
PD1
WR1
WR2
PD2
4c2
CF3
CF2
WR2
6b
CF4
6b
4c1
PD1
4a
PD2
4c2
CF2
CF3
WR2
6b
6a

FIG. 38

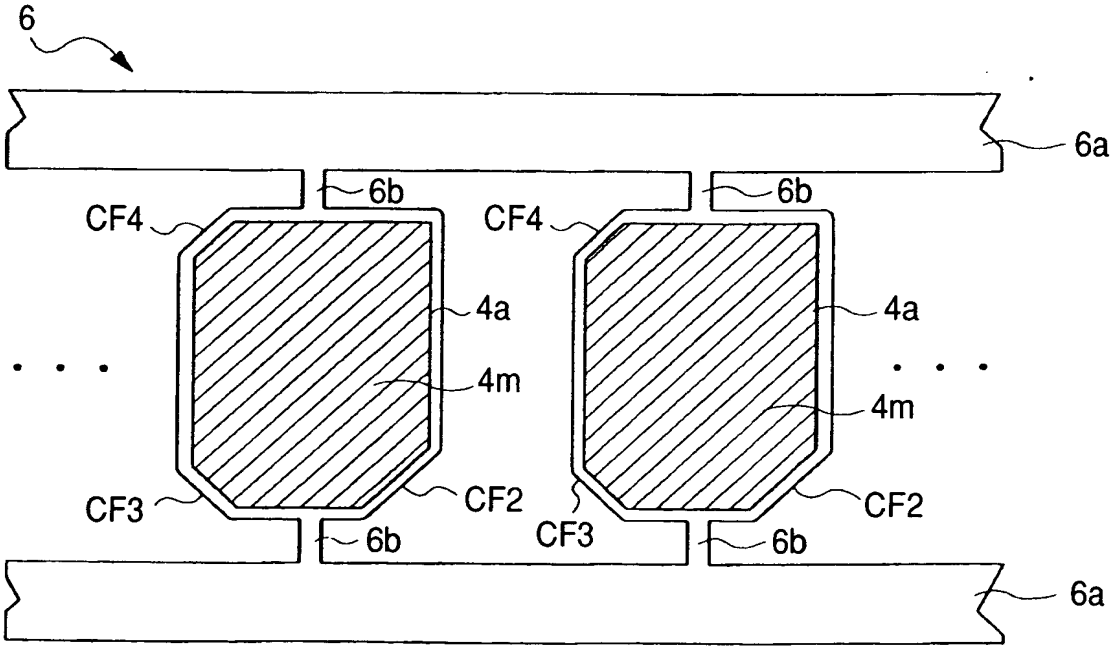

6
6a
6b
CF4
4a
4m
CF3
CF2
6b
6b
CF4
4a
4m
CF2
CF3
6b
6a

FIG. 39

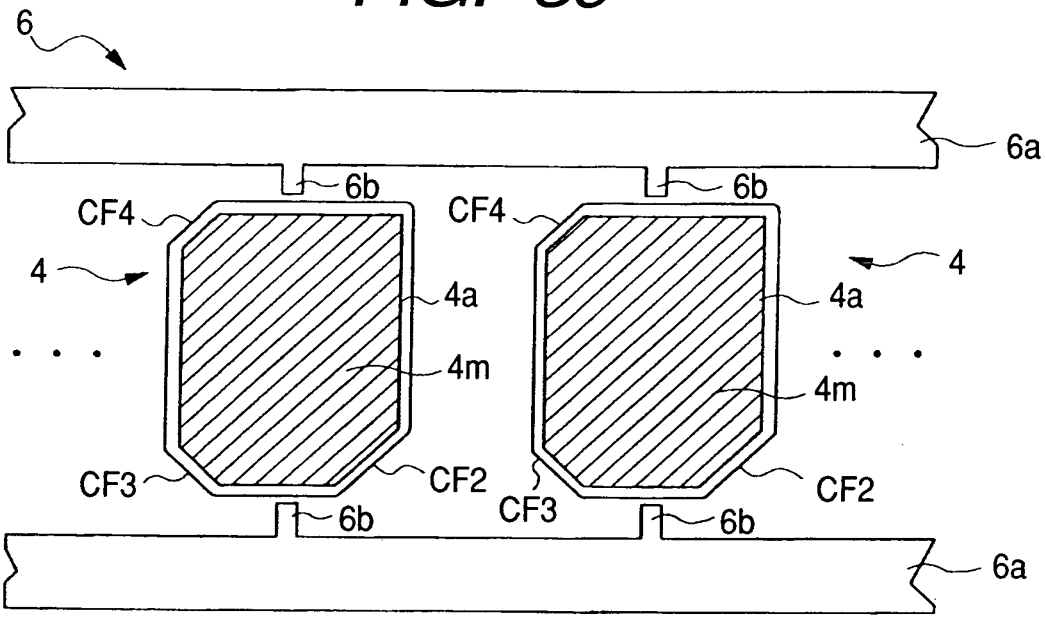

6
6a
6b
6b
CF4
CF4
4
4
4a
4a
4m
4m
CF3
CF2
CF3
CF2
6b
6b
6a

FIG. 40

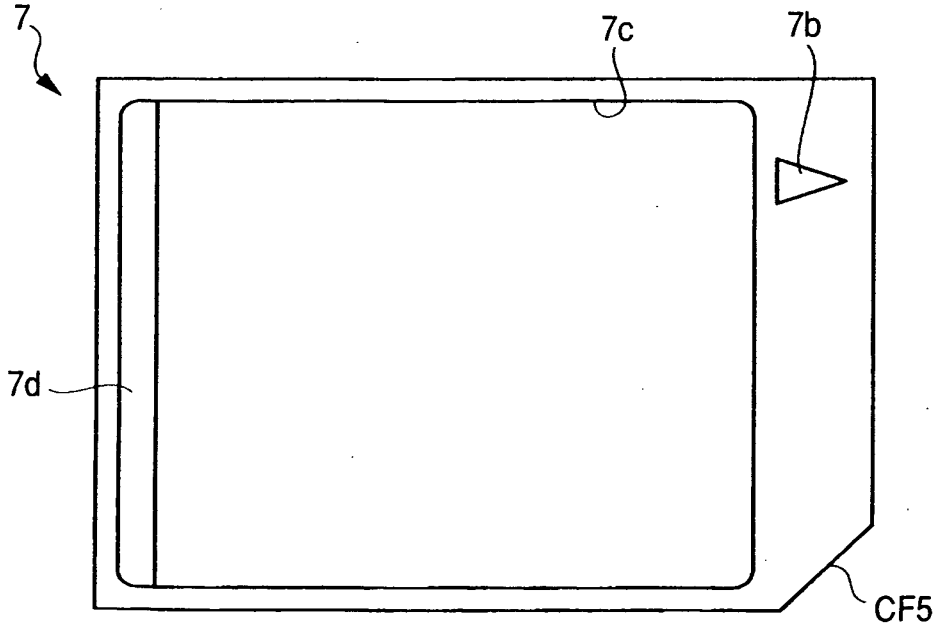

7
7c
7b
7d
CF5

FIG. 41

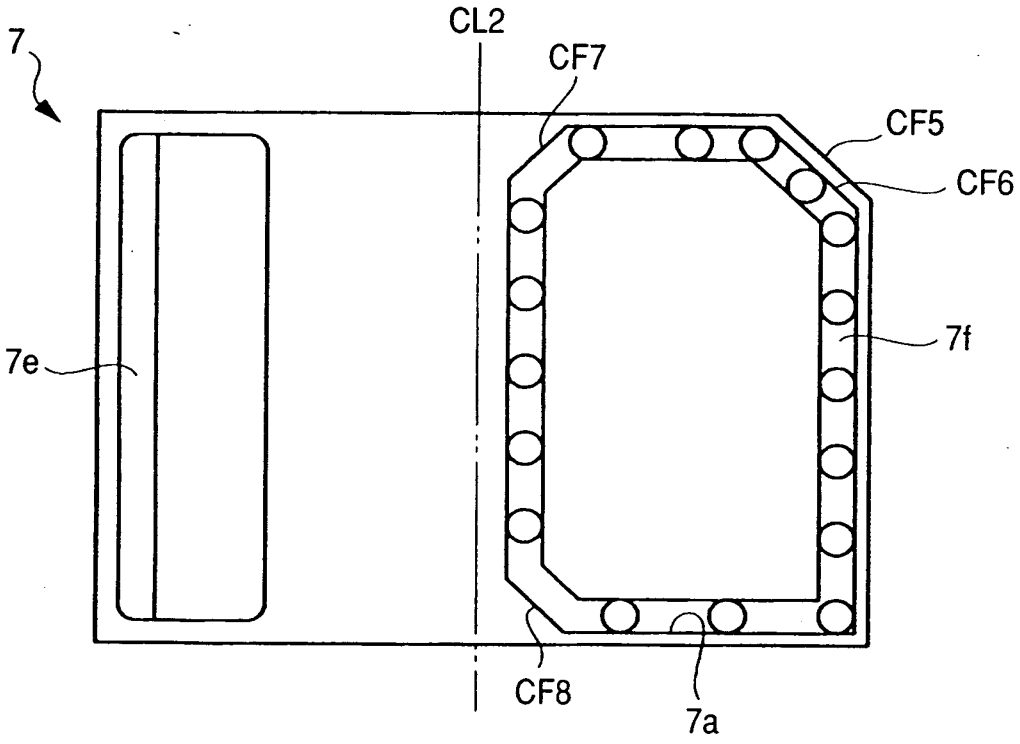


FIG. 42

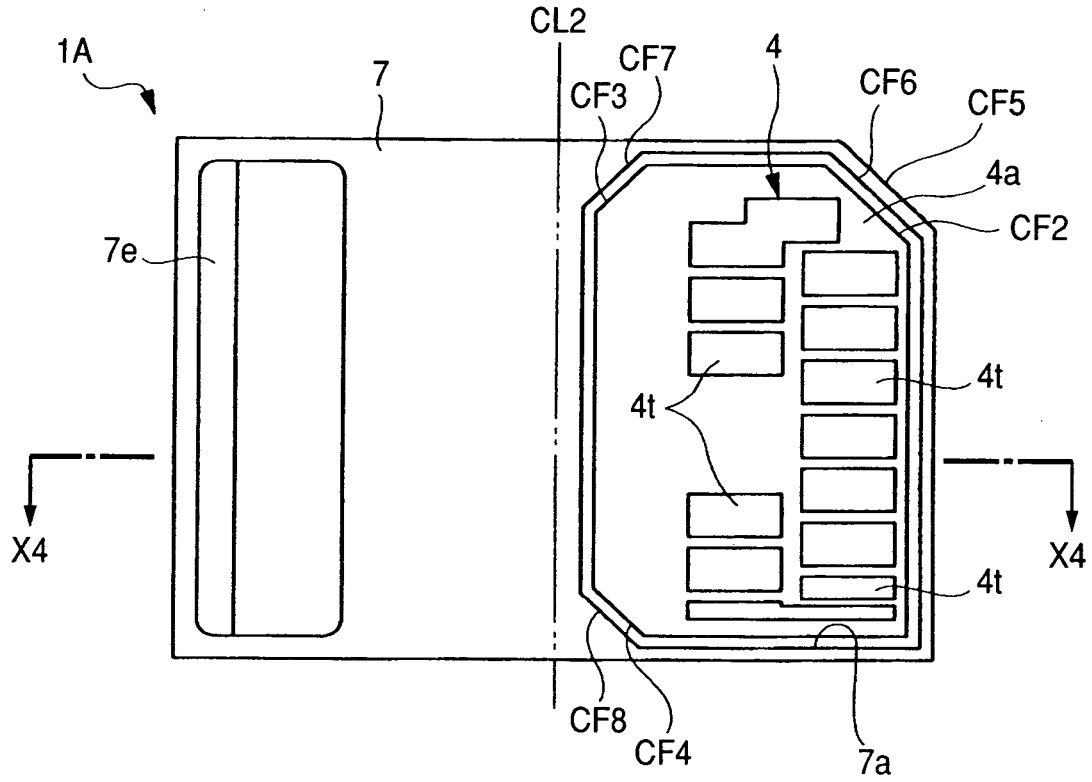

CL2
1A
7
CF7
4
CF3
CF6
CF5
4a
CF2
7e
4t
4t
4t
4t
X4
X4
CF8
CF4
7a

FIG. 43

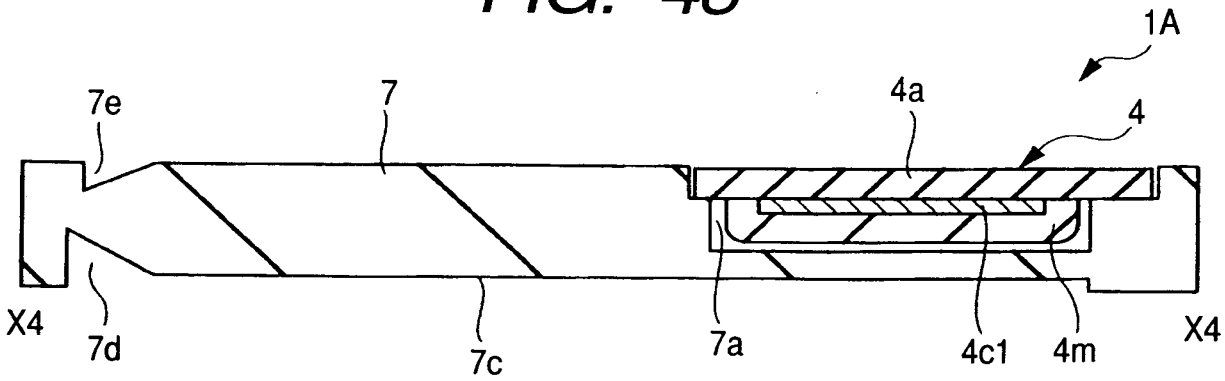

1A
7e
7
4a
4
X4
7d
7c
7a
4c1
4m
X4

FIG. 44

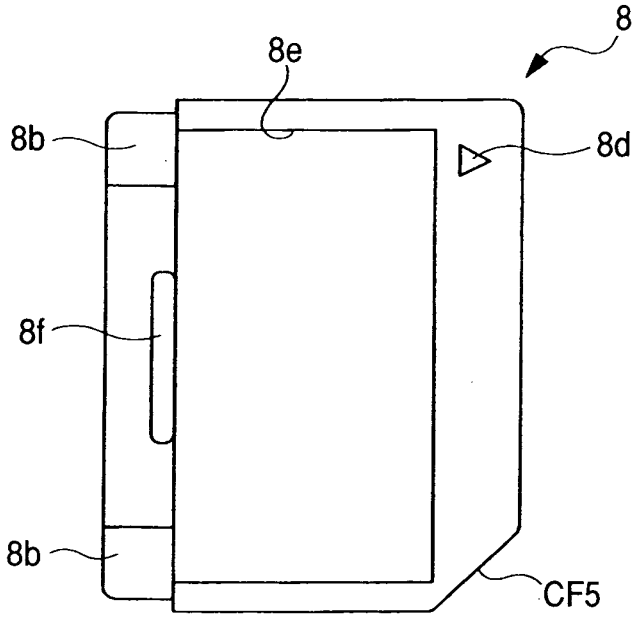


FIG. 45

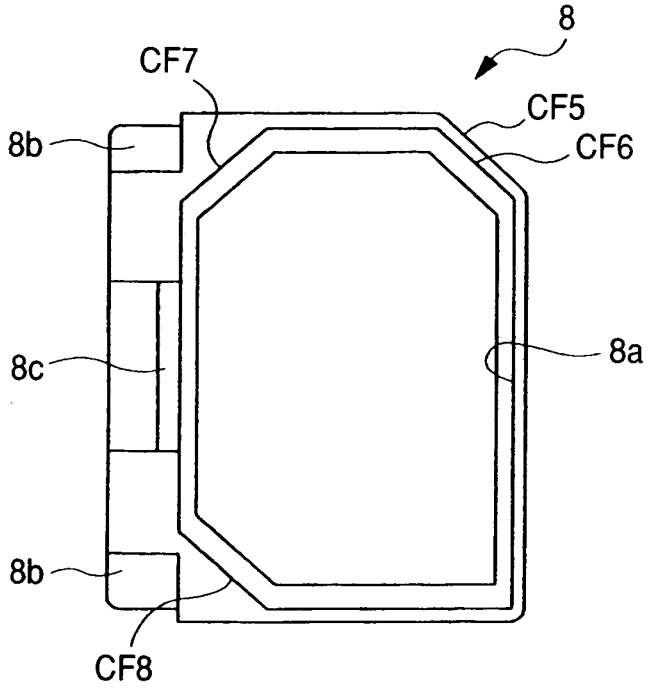


FIG. 46

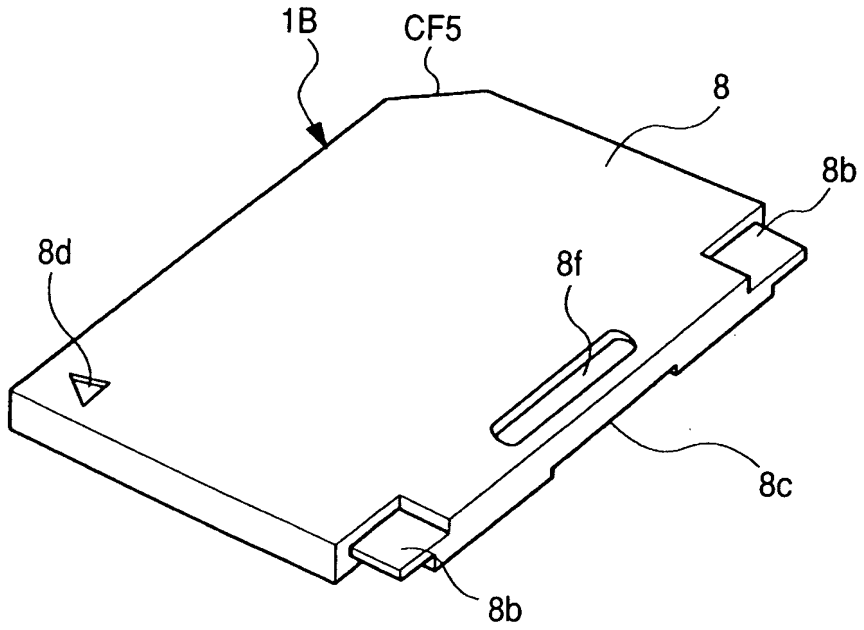


FIG. 47

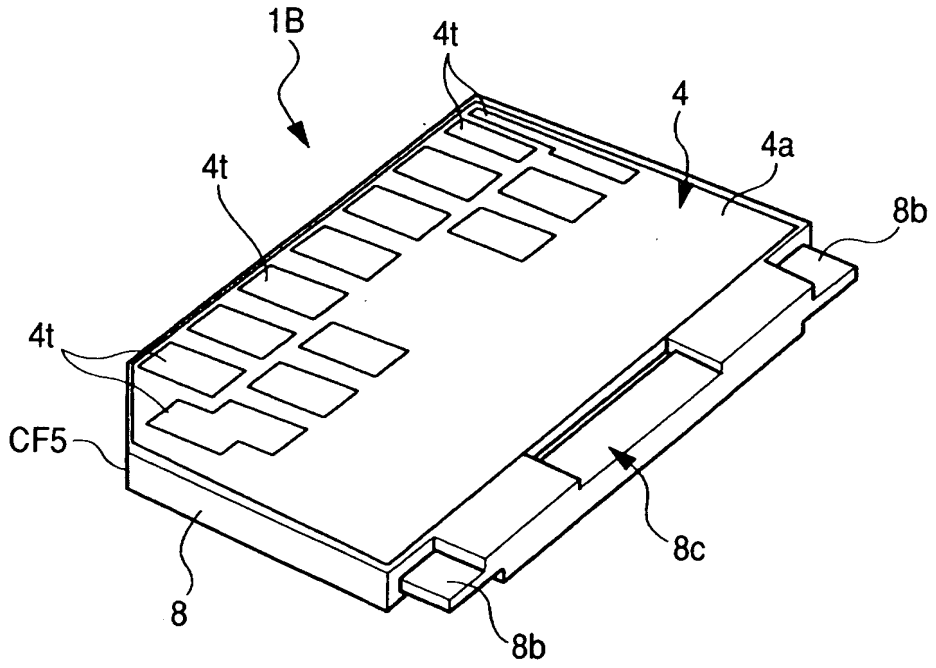


FIG. 48

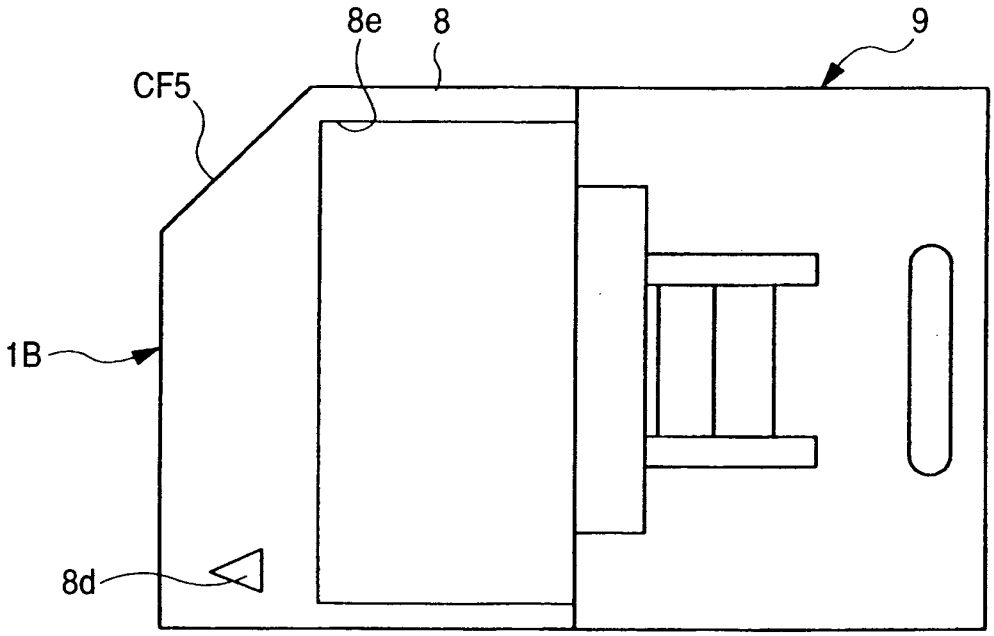


FIG. 49

FIG. 50

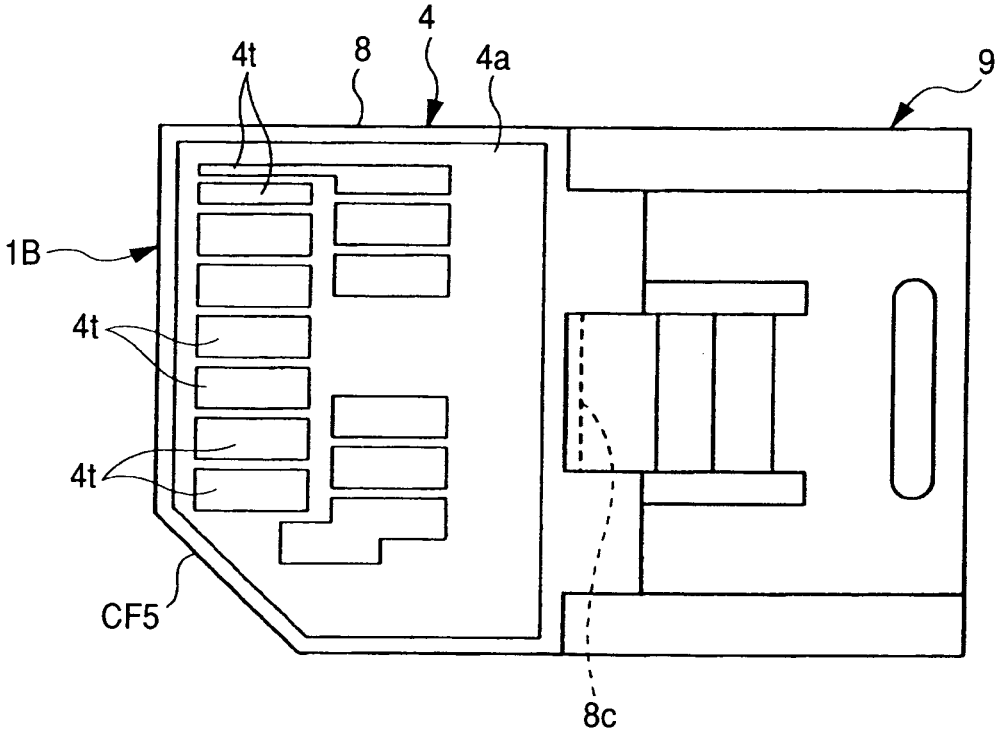


FIG. 51

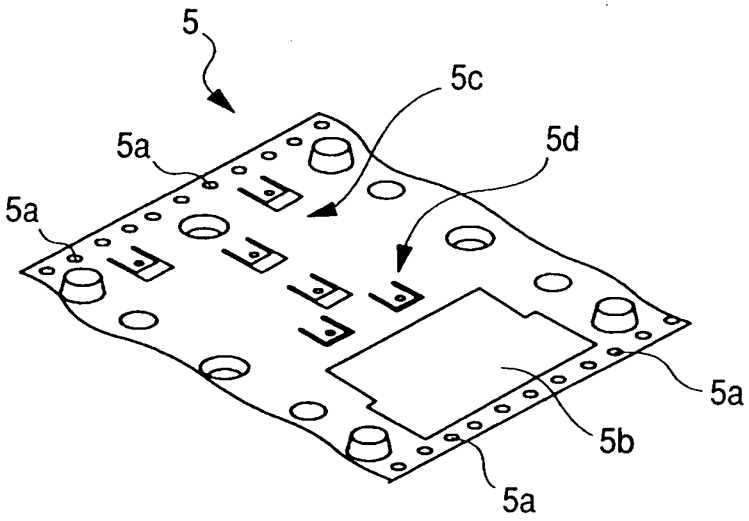


FIG. 52

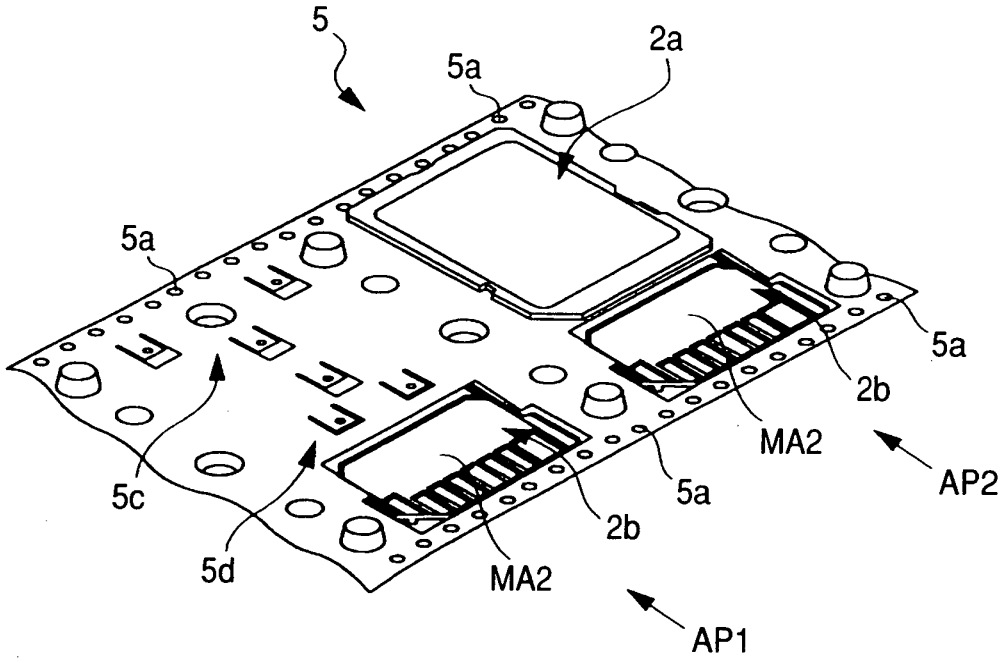


FIG. 53

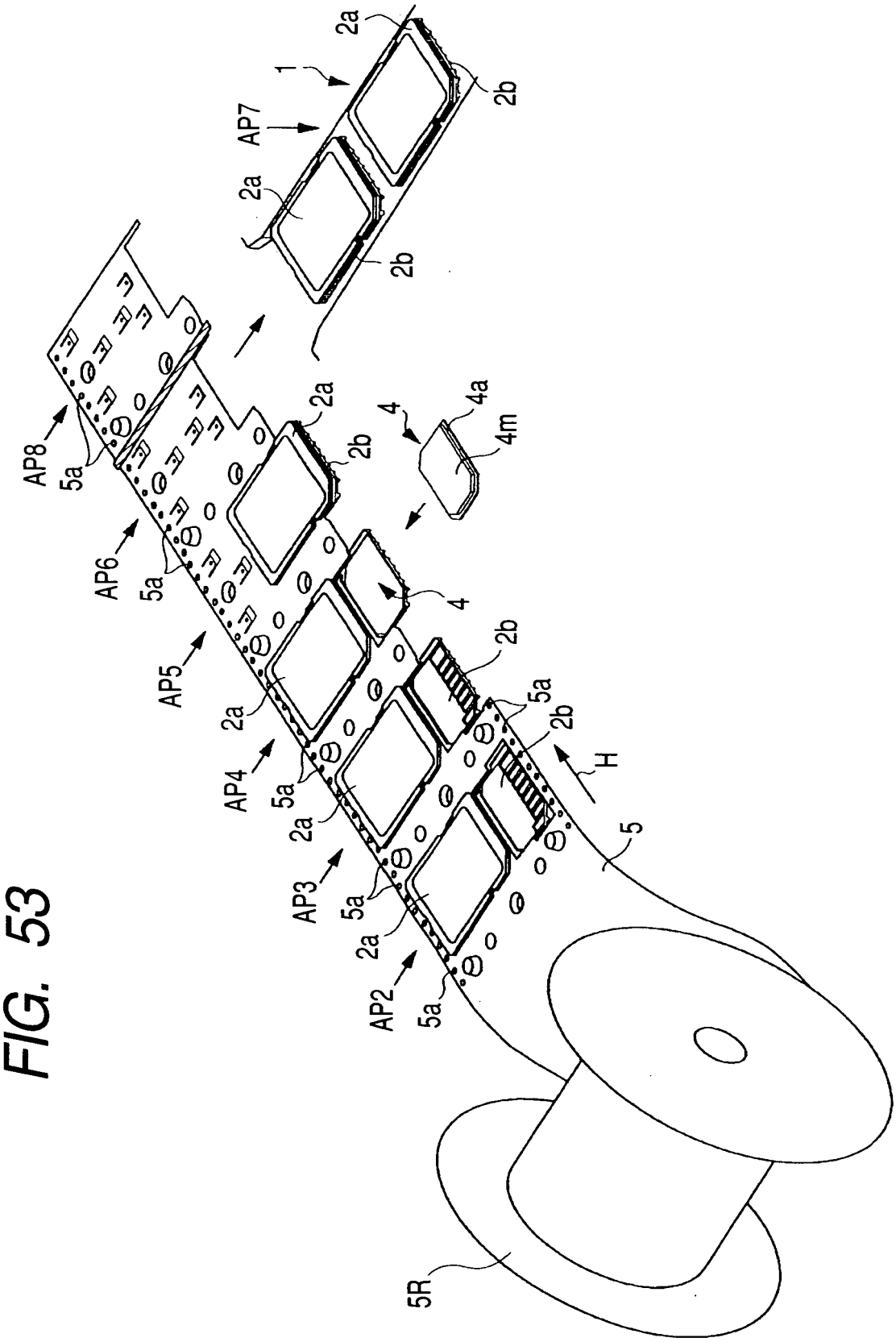


FIG. 54

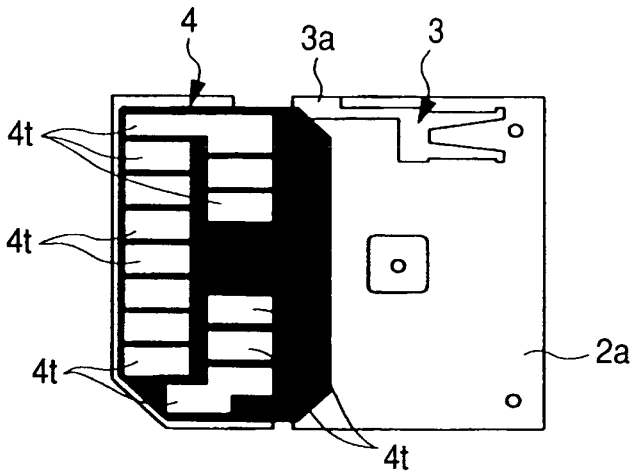


FIG. 55

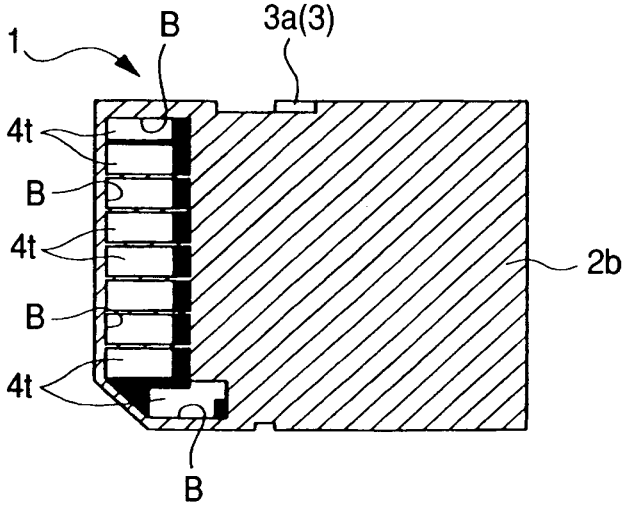


FIG. 56

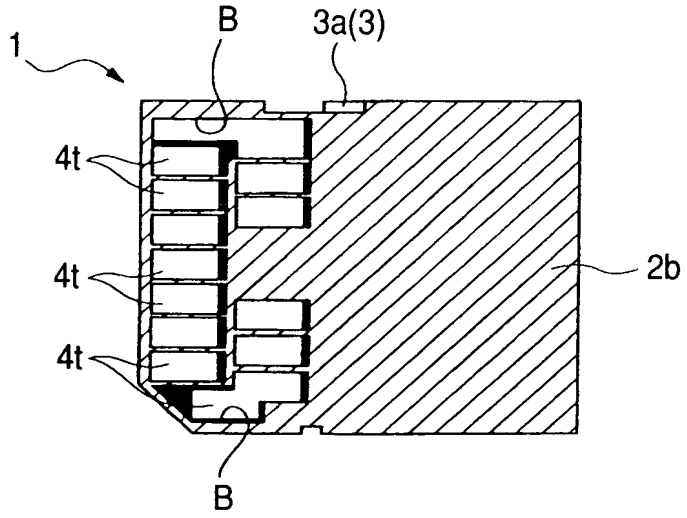


FIG. 57

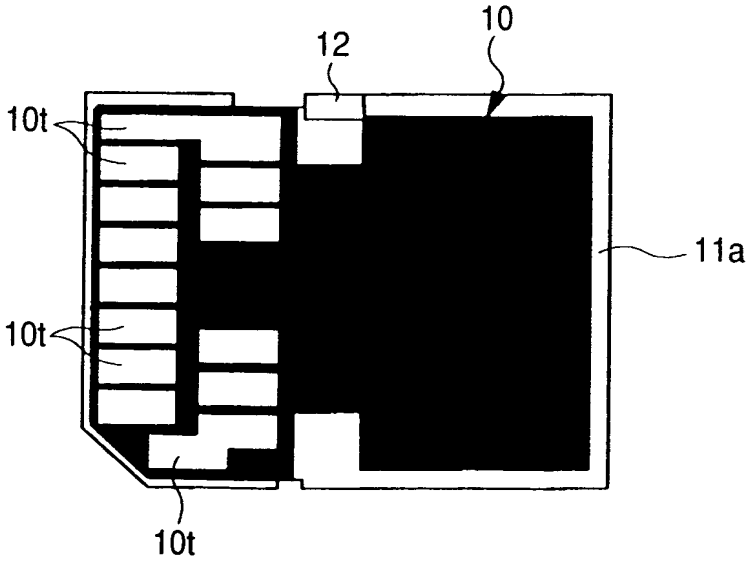


FIG. 58

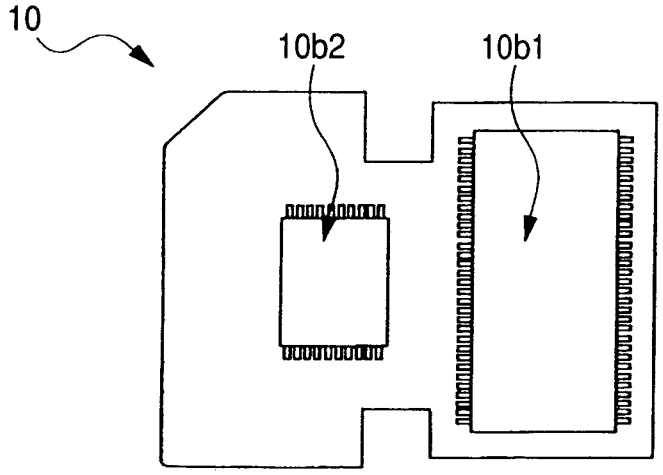


FIG. 59

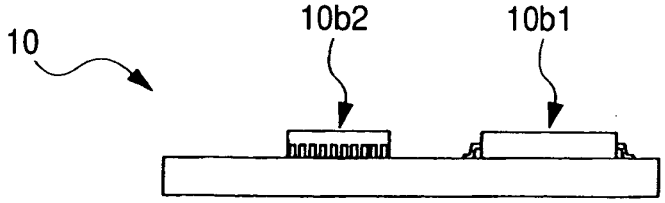
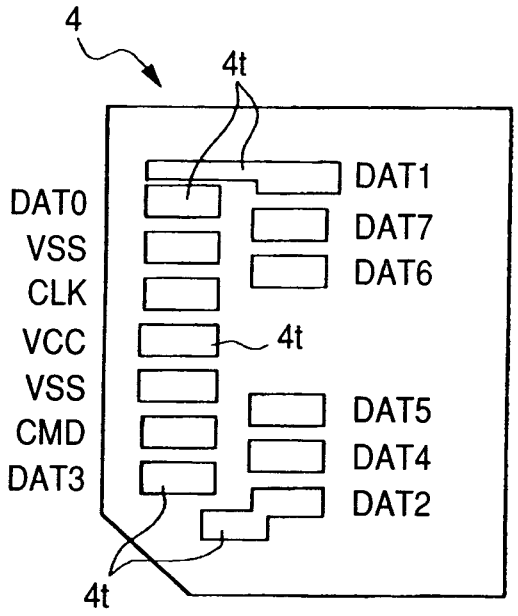
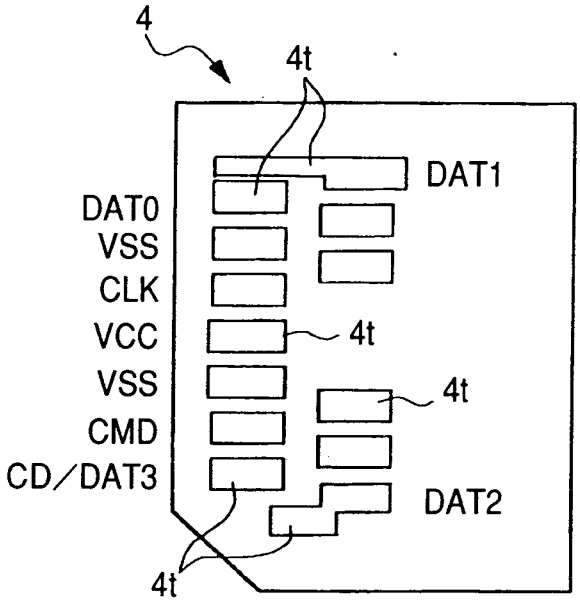


FIG. 60(a)



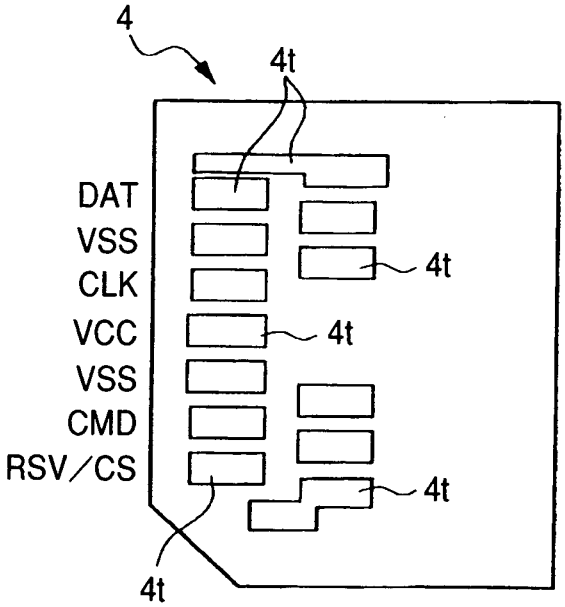
8-BIT MODE PIN ARRAY

FIG. 60(b)



4-BIT MODE PIN ARRAY

FIG. 60(c)



1-BIT MODE PIN ARRAY

FIG. 61

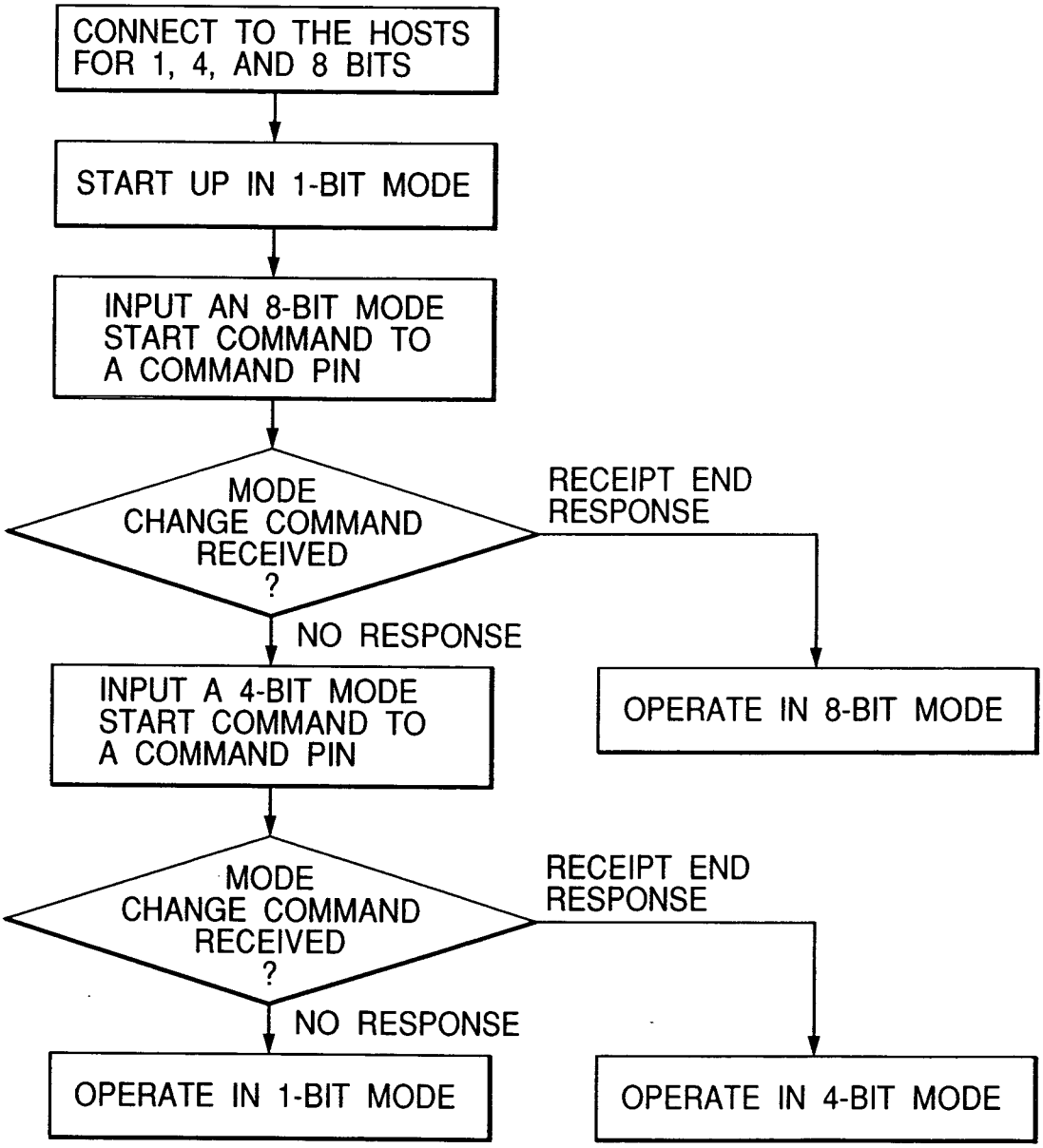
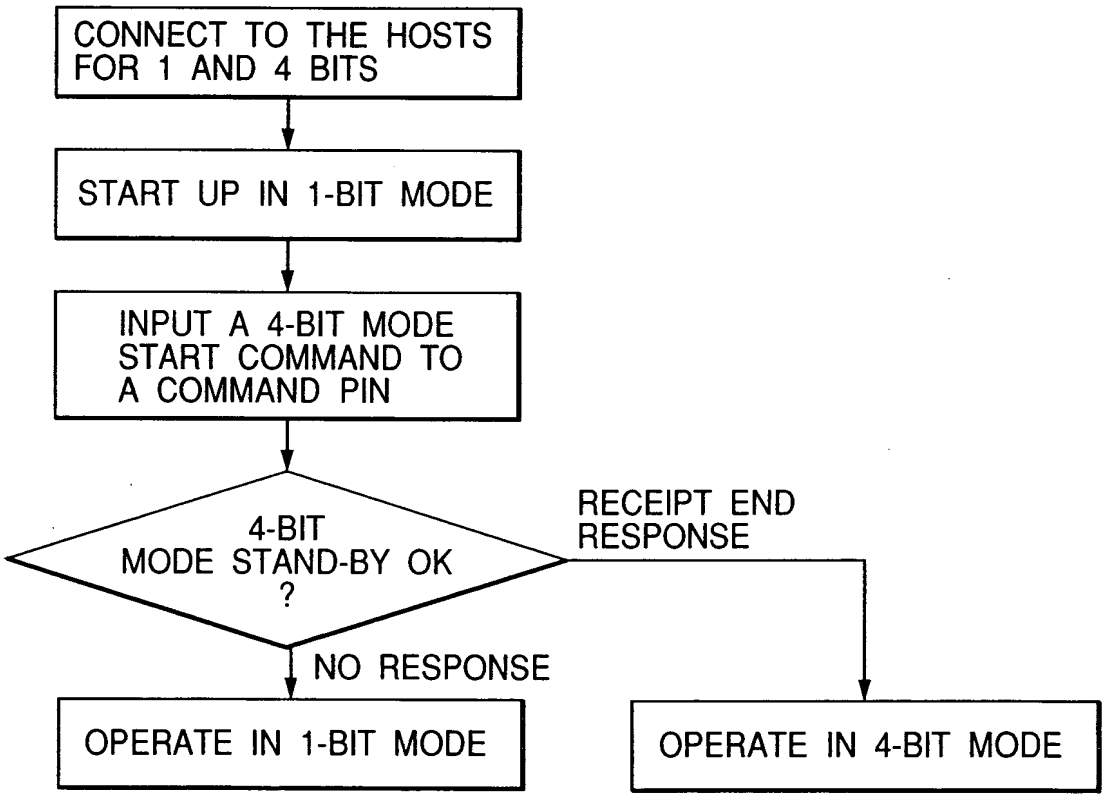

CONNECT TO THE HOSTS FOR 1, 4, AND 8 BITS
START UP IN 1-BIT MODE
INPUT AN 8-BIT MODE START COMMAND TO A COMMAND PIN
MODE CHANGE COMMAND RECEIVED ?
RECEIPT END RESPONSE
NO RESPONSE
OPERATE IN 8-BIT MODE
INPUT A 4-BIT MODE START COMMAND TO A COMMAND PIN
MODE CHANGE COMMAND RECEIVED ?
RECEIPT END RESPONSE
NO RESPONSE
OPERATE IN 1-BIT MODE
OPERATE IN 4-BIT MODE

FIG. 62


CONNECT TO THE HOSTS FOR 1 AND 4 BITS
START UP IN 1-BIT MODE
INPUT A 4-BIT MODE START COMMAND TO A COMMAND PIN
4-BIT MODE STAND-BY OK ?
RECEIPT END RESPONSE
NO RESPONSE
OPERATE IN 1-BIT MODE
OPERATE IN 4-BIT MODE